A Fully-Integrated 1.8-V, 2.8-W, 1.9-GHz, CMOS Power Amplifier

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Abstract

This paper demonstrated the first *2-stage*, 2.8W, 1.8V, 1.9GHz fully-integrated DAT power amplifier with 50Ω input and output matching using 0.18μm CMOS transistors. It has a small-signal gain of 27dB. The amplifier provides 2.8W of power into a 50Ω load with a PAE of 50%.

Introduction

During the last decade, RF CMOS has gone from being an oxymoron to becoming reality as many building blocks of integrated transceivers have been successfully integrated using various silicon-based technologies. Nowadays, RF power amplifiers are mostly implemented as modules using compound semiconductor devices (*e.g.*, AlGaAs, InGaP HBTs) or specialized silicon devices (*e.g.*, LDMOS), both incompatible with today's CMOS processes. These modules also contain a number of discrete passive components that add to the design complexity and thus its sensitivity to component tolerances. Unfortunately, this technology divergence results in further disparities in the supply voltages of different parts of the circuit, as the silicon-based integrated components (*e.g.*, the baseband) have to use a scaled-down supply voltage, while today's PA module needs to use a higher supply voltage to maintain a minimum acceptable output power (P_{out}) and power added efficiency (*PAE*).

The inability to provide fully-integrated solutions for watt-level RF power amplifiers arises primarily from two factors: the high ohmic and substrate energy loss of the on-chip passive components (mainly inductors) and the low breakdown voltage of the active devices. Unfortunately, scaling of integrated circuits to transition to smaller feature sizes and faster speed continues to aggravate the breakdown voltage issue in most device technologies if traditional PA design techniques are to be used, as it limits the output power while the increased passive energy loss reduces amplifier's power efficiency. Some of these loss mechanisms are shown schematically in Fig. 1.

Multiple external components such as bonding wires and external baluns have been used as tuned elements to produce output power levels in excess of 1W using CMOS [1][2] or Si-Bipolar transistors [3]. Alternative technologies with higher breakdown voltage devices or higher substrate resistivity have been used to increase the efficiency and output power of integrated amplifiers. In particular, LDMOS transistors with a breakdown voltage of 20V [4] and GaAs MMICs (monolithic microwave integrated circuit) with semi-insulating substrate [5][6][7] have been used to integrate power amplifiers. To date, the highest power levels achieved with fully-integrated amplifiers in CMOS are on the order of 100mW [8][9] and a fully-integrated solution is still lacking.

In a traditional power amplifier design a resonant LC impedance transformation network similar to Fig. 1 is used to limit the voltage swing seen by the active device and perform the
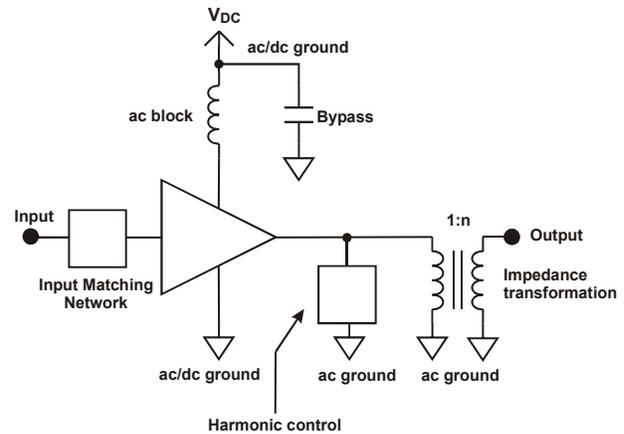

Figure 1. Building blocks of a conventional power amplifier.

impedance transformation. The impedance transformation ratio, *r*, is defined as:

$$r \equiv \frac{R_{load}}{R_{in}} = 1 + Q_l^2 \approx Q_l^2 \qquad (1)$$

where R_{load} and R_{in} are the load and its transformed impedance at port-1, and Q_l is the loaded quality factor of the network. The voltage swing limitations of the active device in combination with desired output power determine R_{in}. A given R_{load} and R_{in} will set *r* and Q_l in (1). This can be used to calculate the value of the inductor, L_p. Knowing L_p, the capacitor value can be selected using the resonant condition.

The passive power transfer efficiency, η, of this network, calculated as the ratio between the input RF power and the RF power delivered to the load can be computed as a function of Q_{ind}, and *r*, as follows:

$$\eta \equiv \frac{P_{out}}{P_{in}} = \cfrac{1}{1 + \cfrac{R_{load}}{\omega L_p Q_{ind}}} \qquad (2)$$

For any matching network, we can define the power enhancement ratio (PER), *E*, as the ratio of the RF power delivered to the load with a transformation network in place, P_{trans}, to the power delivered to the load for the same sinusoidal input voltage source when it drives the load directly, P_{direct}, *i.e.*,

$$E \equiv \frac{P_{trnas}}{P_{direct}} = \frac{P_{direct} \cdot r \cdot \eta}{P_{direct}} = r \cdot \eta \qquad (3)$$

Unlike *r*, power enhancement ratio, *E*, accounts for the loss in the passive impedance transformation ratio and is thus

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particularly important for lossy on-chip passive components in silicon technology.

Using the definitions in (2) and (3), we can find a closed-form solution to calculate the passive network efficiency, η, for a necessary E and available inductor Q_{ind}, as follows:

$$\eta = 1 - \frac{\sqrt{E-1}}{Q_{ind}} \approx 1 - \frac{\sqrt{E}}{Q_{ind}} \qquad (4)$$

Fig. 3 shows plots of η vs. E for several different Q_{ind} for a single section network of Fig. 2. For instance, with a PER of 50 and an inductor Q_{ind} of 10, the matching network alone will have a maximum passive power efficiency of around 30%. This does not include any loss in the active device, the driving network, or the external connections. We can also see in the Fig. 2 that for a given inductor quality factor, Q_{ind}, there is an upper bound on the maximum achievable PER, E, where the passive efficiency, η, becomes zero.

This approach can be extended to multisection transformation networks [11]. In principle, such multi-section networks have a lower loss for high PER compared to a single section. However, it requires a more complex layout and some of its inductors will have a very large range of reactances compared to a single section. This results in a lower overall quality factors, Q, for the network. For example, we can show that with a PER of 50 and an inductor quality factor, Q_{ind}, of 10, the best matching network will have 3 LC-sections and will have a maximum passive efficiency of around 60%. Again, this figure does not include any loss in the active device, the dc feeds, or the external connections.

Equation (4) has important implications regarding the necessary reactance, transformation efficiency, and the PER. In particular, the inductor reactance necessary for this type of matching network with a single-section decreases rapidly as the desired PER is increased. More importantly, the transformation efficiency, η, also decreases quickly with higher PER, as can be seen in Fig. 2. In a multi-section approach, the loss is improved significantly compared to the single-section network, but still increases with higher PER. PA designers have long understood this trade-off by intuition and experience. The low Q passives currently available on chip fundamentally limit achievable power efficiencies at the 1-Watt level. No amount of complexity in an LC transformation network can overcome this, making it necessary to pursue alternative approaches hence the introduction of distributed active transformers (DAT).

In the past, we have demonstrated a single-stage fully integrrated distributed active transoformer (DAT) [10]. In this paper, we report the first *2-stage* distributed active transformer power amplifier capable of operating on a single cell battery. This design demonstrates the highest gain, PAE, and output power demonstrated in a fully-integrated CMOS PA to this date. The two gain stage DAT design improves the power gain and hence the overall power added efficiency (PAE) of the amplifier. The DAT combines in series several low-voltage push-pull amplifiers efficiently to produce a larger output power while maintaining a 50Ω match. Furthermore, it desensitizes the operation of the amplifier to the
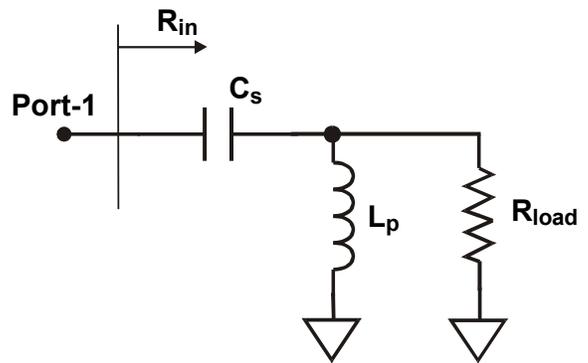

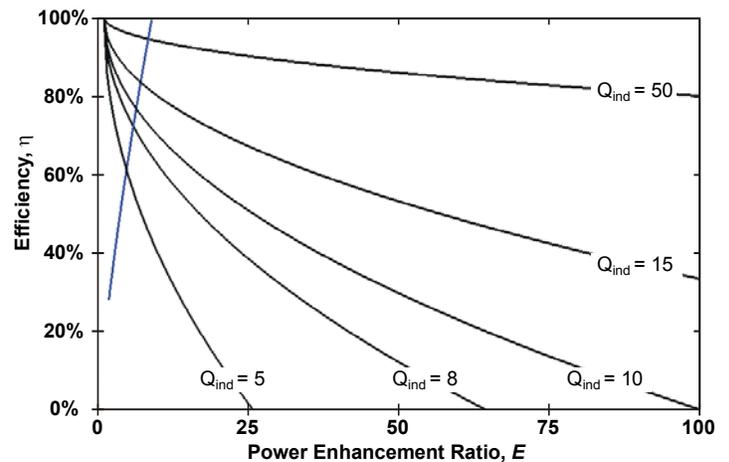Figure 2. deal resonant LC impedance-transformation network

Figure 3. Efficiency vs. PER for different inductor Q in a single-section resonant impedance transformation network.
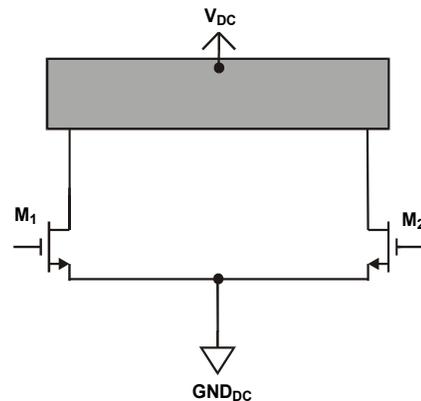

Figure 4. Basic balanced drive stage

inductance of bonding wires and makes the design more reproducible.

The basic building block of the DAT is a push-pull amplifier shown in Fig. 4. This topology creates a virtual ac ground at the power supply and ground. Because these virtual ac grounds are created by symmetry, they are inherently low-loss and low-impedance. The connection from these ac virtual grounds to the

positive supply and ground eliminates the loss caused by the RF signal at the fundamental frequency and odd harmonics going through lossy supply lines. They also avoid the need for a lossy on-chip choke inductor. The connection from these ac virtual grounds to the positive supply and ground will carry only current at dc and even harmonics, thus eliminating the loss caused by the RF signal at the fundamental frequency and odd harmonics going through lossy supply lines. Furthermore, this effect desensitizes the operation of the amplifier to the inductances of bonding wires making the design more reproducible. It also eliminates the need for a large on-chip bypass capacitor on the supply.

Figures 5a and 5b show a push pull amplifier illustrating the impedances seen by even and odd harmonics, respectively. The differential output signal, V_1-V_2, does not contain any even harmonic components due to symmetry. The elimination of the even harmonics, especially the 2*nd*, by the circuit symmetry allows for the use of a lower loaded Q – and therefore lower loss – resonant circuit at the drain for harmonic suppression as it only needs to suppress odd harmonics.

If switching modes of operation are desirable, the differential symmetry of this topology provides high impedances, $\sim 2Z_{Vdd}$, at each even harmonic to the transistor drains regardless of the impedances of the output resonant network, Z_l, at these frequencies, as shown by Fig. 4a. The transistor drain impedances at odd harmonics will be Z_l, as can be seen in Fig. 4b and the following equations:

$$Z_{even} = Z_l + 2Z_{vdd}$$
$$Z_{odd} = Z_l$$

<div align="right">(5)</div>

By providing a short circuit between the drains at each odd harmonic using a simple parallel LC tank tuned to a frequency slightly above the fundamental frequency, the drain impedance will be inductive at the fundamental and will be small at odd harmonics and large at even harmonics. If transistors are driven into saturation, these impedances shape the drain waveforms to perform the high efficiency operation.

The differential push-pull inductor is implemented using an on-chip slab inductor, which present a higher Q when compared to conventional low impedance single-turn spiral inductors.

Distributed active transformer (DAT) is a means to create low-loss, low-impedance virtual ac grounds while using several power amplifier blocks simultaneously. For instance, Fig. 4 shows the primary circuits with four push-pull power amplifiers and eight gain stages. The DAT allows the creation of virtual ac grounds without having to connect together the sources of the pair of transistors of each push-pull amplifier, as shown in Fig. 4. With slab inductors, this connection is physically impossible due to the large distance between the sources of transistors on two ends of the slab. If a long metal line is used to connect the sources of this pair of transistors, the inductance of this metal will be comparable to that of the drain slab inductor and the resulting source degeneration inductor will seriously degrade the amplifier performance.
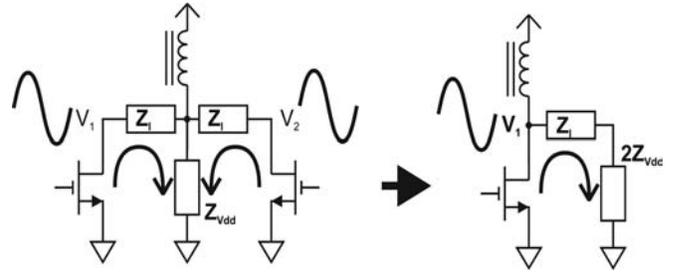

Figure 5. Equivalent circuit for a) odd and b) even harmonics.

Ac virtual grounds for the fundamental and all odd harmonics can be created in the corner points of the circular-geometry by connecting together the sources of the transistors of the adjacent push-pull amplifiers. By driving these transistors in opposite phase, their source currents, which belong to different push-pull amplifiers, have the same amplitude and the opposite phase and therefore cancel each other.

The power combining for the various push-pull stages is accomplished by introducing a single-turn metal loop to act as a magnetic pick-up of the output power, as shown in the Fig. 6. The $n/2$ push-pull amplifiers, (four in this example), conduct identical synchronized ac currents at the fundamental, inducing corresponding ac magnetic fields in this secondary loop. The internal metal loop harnesses the induced magnetic field to generate a voltage between its terminals equivalent to the sum of the differential voltages of the $n/2$ push-pull amplifiers. This DAT architecture results in a simultaneous 1:n impedance transformation and n transistor series power combining.

A 1.8V, 2.8W, 1.9GHz two-stage fully-integrated distributed active-transformer switching power amplifier has been fabricated and measured using 0.18μm CMOS transistors. The substrate in this process has a resistivity of 8Ω.cm. The PA has a small signal gain of 27dB and a compressed power gain of 17dB at peak efficiency. It achieves a peak PAE of 50% including all the power losses in the circuit with single-ended 50Ω source and load resistance. Fig. 7 shows the measured output power P_{out}, the power gain, and the overall PAE as a function of the input power. The microphotograph of the chip can be seen in Fig. 8.

All the pins including the input and output are wire bonded on a printed circuit board. The DAT power amplifier is not sensitive to the exact length of these wirebonds. The bonding wire power loss is included in the amplifier's measured performance and is not de-embedded. Table 1 summarizes the results showing that this design provides the highest PAE and P_{out} in a fully-integrated CMOS setting.

Table 1. Measurement Results

Center Frequency	1.9GHz
Maximum Pout	2.8Watt
Peak PAE	50%
Small signal gain	27dB
Compressed gain	17dB
Input impedance	50Ω
Output Impedance	50Ω
Supply voltage	1V-1.8V
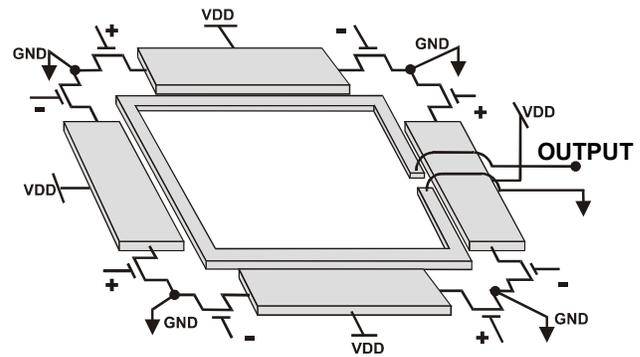
Figure 6. A DAT with 8 transistors.

Acknowledgments:

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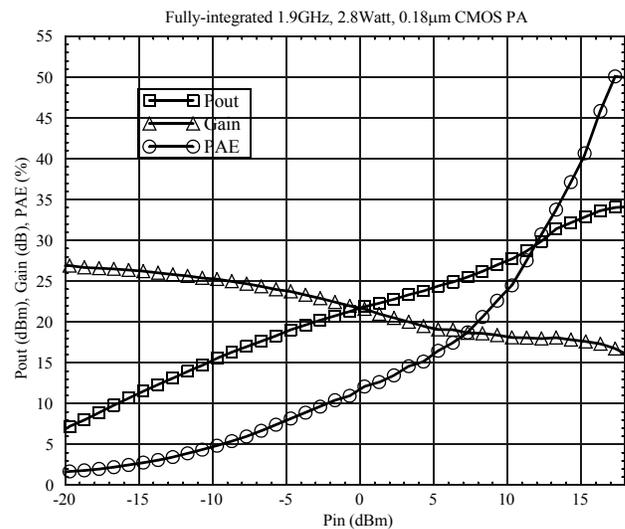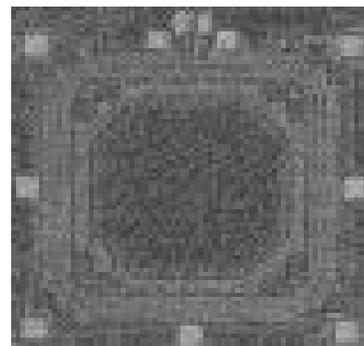
Figure 7. The measured gain, PAE, and output power of the 0.18um CMOS power amplifier.

Figure 8. Die photo of the chip.