10.4 Differential 4-tap and 7-tap Transverse Filters in SiGe for 10Gb/s Multimode Fiber Optic Link Equalization

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Ethernet and Fibre Channel are the two most prevalent standards used today in LAN and SAN environments and in these, the use of multimode fiber links dominates. The distances for wiring premises now reach 550m. The laser-driven gigabit LAN links expose the need for extension of the achievable distances in those standards which become impractically short at 10 to 40Gb/s.

In a multimode fiber (MMF), multiple modes are allowed to propagate. All modes propagate at different speed, resulting in signal distortion which becomes more severe with longer distances. One way to compensate for this modal dispersion, and still keep the economic advantage of MMF over single mode fiber (SMF), is to equalize the received signal with a finite impulse response (FIR) filter, as shown in Fig. 10.4.1. A transverse filter is one of the possible implementations of this FIR filter.

In low-speed applications, the equalizer is digitally implemented using shift registers or memory as delay elements. As the signal speed increases, analog implementations have been used such as CCD, and SAW switched capacitor, and g_m-C ladder filters. For data rates above a few Gb/s, RF techniques are necessary to implement a transversal filter. It is proposed to use transmission lines both as delay elements and signal combining devices in high-speed transversal filters [1][2] in a manner similar to traveling-wave amplifiers.

In this work, integrated transverse filters are designed to operate at 10Gb/s based on this architecture. The schematic of the prototype transversal filters are shown in Fig. 10.4.2a. The input signal is fed to multiple gain stages through the input transmission lines and the weighted outputs are combined through the output transmission lines. Both transmission lines generate the required delays and are terminated at the dummy ends. The filters are designed to implement fractional-spaced equalization, and thus have a 50ps delay per stage. The transmission lines are too long to be implemented on-chip as microstrip lines or coplanar waveguides. Therefore, they are implemented as LC ladders consisting of spiral inductors and MIM capacitors. To overcome the difficulties in RF grounding and substrate modeling, differential topologies are used in the LC transmission lines as well as gain stages.

The gain stage schematic is shown in Fig. 10.4.2b. The core of the circuit is a differential amplifier (Q_1 and Q_2). The weight is implemented using the tail current source I_w (a current mirror in the prototypes), having a better linearity than a cascode structure and is less sensitive to the control voltage. The sign of the weight is implemented using two pairs of current-steering transistors (Q_3 , Q_4 , Q_5 and Q_5). The control signals of these switches (S_1 and S_2) are analog voltages selected by a single digital sign bit. Because the output taps are always connected to the collectors of an "ON" transistor and an "OFF" transistor, there is no loading variation on the output transmission lines. The differential input signals are buffered using emitter followers (Q_{b1} , Q_{b2} , I_1 and I_2). Buffering reduces the loading and thus improves the phase response linearity on the input transmission lines. Further, the

buffers are biased with constant currents, so the parasitic capacitances of $Q_{\rm b1}$ and $Q_{\rm b2}$ do not change with the weight (I_w) . Hence, there is no loading variation on the input transmission lines.

Two prototypes are designed and fabricated, with 4 and 7 taps, respectively. Figure 10.4.3 shows the measured response of the 7-tap filter to a 2.5Gb/s square wave when only one of the coefficients is non-zero. The plots show an approximate delay per stage of 50ps. Figure 10.4.4 shows the frequency response of each stage of the 4-tap filter. The gain drop at low frequencies is due to the bandwidth limit of the hybrid junction coupler in the measurement setup, used to generate the differential input signal. From the phase responses, the group delay of each stage is extracted. The gain of each stage is a linear function of the weight current I_w , as shown in Fig. 10.4.5 for stage 3 of the 4-tap filter. The phase response for any stage does not change with weights. The signals through different taps are also shown to add linearly.

To test the actual equalization capability of the filters, a setup similar to the application environment shown in Fig. 10.4.1 is used. 800m, $50\mu\text{m}$ non-compliant NGMMF fiber is used to distort the signal. The test pattern is set to 2^{31} -1 PRBS pattern at 10Gb/s. This generated a signal with 5.0dB of ISI at the input of the filter. After equalization by the 7-tap transversal filter, the equalized signal has a residual ISI of 1.38dB. The equalization operation also decreases the jitter in the signal from 62ps to 38ps. Overall BER improves from 10^{-5} to less than 10^{-12} . Figure 10.4.6 shows the resulting eye diagrams, before and after equalization using the 7-tap filter.

These chips were fabricated in a 0.18µm BiCMOS SiGe process with $f_\tau=120 GHz.$ The chip areas are 1.0mm x 1.7mm and 1.0mm x 2.5mm for the 4-tap and 7-tap filters, respectively not including the pad cage. Figure 10.4.7 shows a micrograph of the 7-tap transversal filter. The power dissipation is typically 4.5mW per stage plus 2mW per active coefficient.

Acknowledgements

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References

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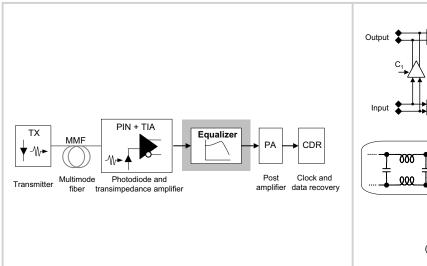


Figure 10.4.1: Components in a multimode fiber link, with the equalizer on the receive side.

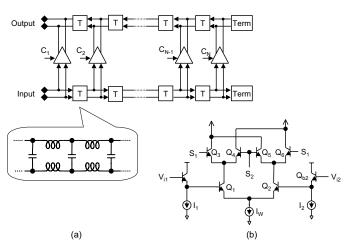


Figure 10.4.2: (a) Schematic of differential transversal filters; (b) implementation of gain stages.

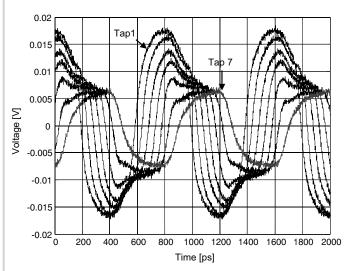


Figure 10.4.3: Square wave response of each stage in the 7-tap TF.

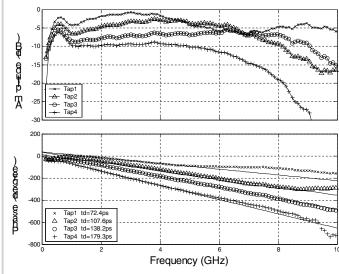


Figure 10.4. 4: Frequency response of each stage in the 4-tap TF.

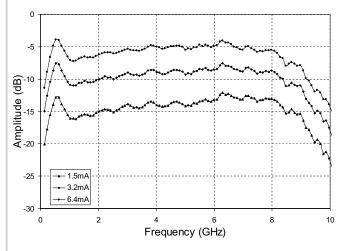


Figure 10.4.5: Frequency response of stage 3 in the 4-tap TF with different tap weights.

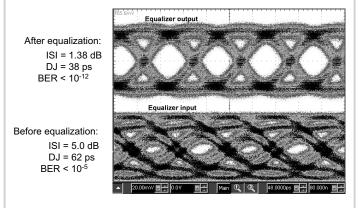


Figure 10.4.6: Eye diagrams before and after equalization for a 500m MMF.

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