A Wideband CMOS Linear Digital Phase Rotator

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Abstract-**This paper presents a 10-bit wideband Cartesian phase rotator with a novel linear digital VGA implemented in a 0.13um CMOS process. The VGA topology is robust to device modeling uncertainties and PVT variations. The system provides 7.8dB voltage gain with -3dB bandwidth of 7.6GHz. A maximum phase error of 2º has been achieved for a phase shifting range of 360º with 32 phase steps of 11.25º. The capability to compensate for mismatched quadrature inputs is also demonstrated.**

I. INTRODUCTION

The beam forming and electrical steering capabilities of a phased array system depend mainly on the phase shifting resolution. Various on-chip phase shifters have been reported in the past [1]-[8]. In general, a phase shifter functions as an adjustable delay element and can be classified into two categories depending on whether the signal is broadband or narrowband in nature.

Phase shifting of a broadband signal needs to provide a constant group delay over the signal bandwidth. Reflective-type couplers [1][2], all pass/low pass/high pass filters [3][4], and true/synthetic transmission lines [5][6] have been traditionally implemented for this application. However, for a narrowband system, the true time delay can be approximated as a phase shift at the center frequency leading to simplified phase shifting block design [9]. The phase shift for the narrow band signal can be implemented in either the signal path or in the LO path. While the signal path phase-shifting architecture reduces the number of RF blocks, the nonlinearity and noise performance of the phase shifter is critical in this scheme. Moreover, the phase shifter needs to maintain a constant gain for its phase shifting, which adds to the design challenges. The LO path phase shifting architecture circumvents these problems. Its single tone nature as well as the filtering after mixing reduces the linearity requirement, and its large signal amplitude enables more tolerance to noise. Furthermore, the sensitivity of mixer gain to the saturated LO signal amplitude is low, which reduces the constant gain requirement for the phase shifter.

This LO phase shifting scheme can be achieved by generation and selection of multiple-phase LO signals [7]. Putting aside the difficulty of multiple-phase VCO design, its distribution network has disadvantages such as area inefficiency, signal crosstalk, signal loss, and delay mismatch.

An alternative LO path phase shifting approach avoids these problems by using phase rotator which rotates the LO phase locally [8]. In a phase rotator, a pair of variable gain amplifiers (VGA) set the relative weights of the in-phase (I) and quadrature (Q) components separately with the combined outputs yielding the desired signal (Fig.1). RC-CR pairs, RC polyphase networks, or frequency dividers can be used to generate the I and Q. However, both amplitude and phase mismatches are inevitable for such quadrature generation circuits during wideband operation. This results in phase errors which cannot be easily calibrated by traditional phase rotators. Moreover, conventional designs control the VGA gain in an analog fashion by adjusting the biasing currents or by switching the load. These topologies rely heavily upon the modeling accuracy of both active and passive elements. Furthermore, they fail to provide constant output DC voltage or the same -3dB bandwidth across all phase shift settings. However, these properties are particularly important in a broadband system, where DC coupling between stages and constant attenuation of high order LO harmonics are desired.

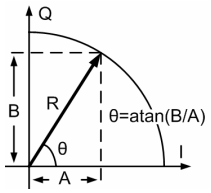

Fig. 1. Vector Diagram of Cartesian Phase Interpolating

The linear digital Cartesian phase rotator proposed in this paper addresses all the aforementioned issues for the LO phase shifting scheme. It adopts a novel scalable VGA design which is insensitive to modeling uncertainties and PVT variations. Moreover, by implementing a 10 bit digital control, the phase rotator can significantly decrease the interpolating phase errors due to input I/Q mismatches. This functionality effectively extends the bandwidth of the entire beam forming system in the wideband phased array application.

This paper is organized as following. Section II introduces the definitions of phase error and phase resolution. The phase rotator design and the proposed digital linear VGA circuit is discussed in Section III. The measurement results are presented in Section IV.

II. PHASE ERROR AND PHASE RESOLUTION

The target phases are normally 2^N discrete phases equally spaced between 0º and 360º. Due to the limited DAC bits, phase rotator produces finite discrete phases from which the best matched phases are selected as the interpolation results. Similar to the definitions of integral nonlinearity (INL) and differential nonlinearity (DNL) in digital-to-analog converters, integral phase error (IPE) and differential phase error (DPE) can be defined for a phase rotator in eq. 1.a and 1.b (Fig.2).

$$IPE(n) = P_i(n) - P_{ideal}(n) = P_i(n) - (n-1)\times 360^0 / 2^N \quad (1.a)$$

$$DPE(n) = (P_i(n) - P_i(n-1)) - 360^0 / 2^N \quad (1.b)$$

$$where\ P_i(n) = InterpolatedPhases(n);$$
$$P_{ideal}(n) = Ideal\ Phases(n) \qquad n \in [1, 2^N]$$

If both the maximum IPE and the maximum DPE are smaller than $360^0/2^{N+1}$ (half of the ideal phase step), the phase rotator will achieve N bit phase resolution. Defining phase error as such, we can systematically characterize the phase rotator.

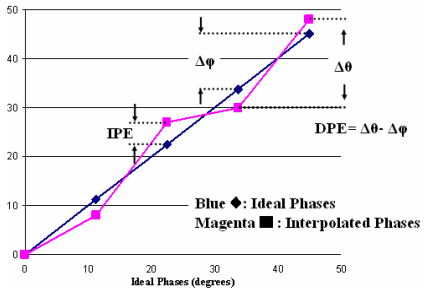

Fig. 2. Definition of IPE and DPE

In a Cartesian interpolation scheme, a phase rotator with an M-bit DAC quantizes the I and Q axes each by $M/2$ bits to produce $(2^{M/2}-1)\times(2^{M/2}-1)$ points on the constellation plane. Given the tolerance on the amplitude variation, the best-matched phases can be found for every ideal $360^0/2^N$ step (Fig.3). For a given phase shift resolution (bit N), the systematic phase error due to quantization effect can be decreased by increasing the tolerance on amplitude variation and/or by increasing the number of bit M in the DAC. (Fig. 4).

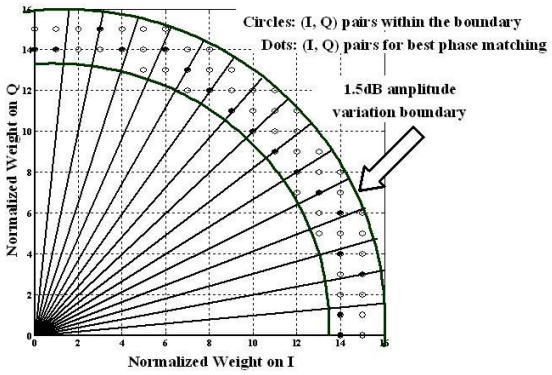

Fig. 3. 10 bit Cartesian Phase Interpolating, M=10 and N=6

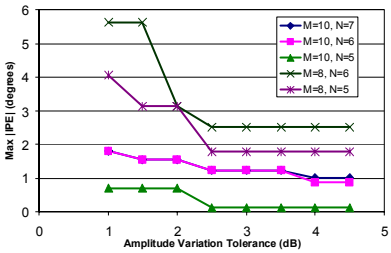

Fig. 4. Relation between Max |IPE|, Amplitude Variation Tolerance, Phase Rotator Bit M, and Target Phase Bit N

The phase rotator design in this paper implements a VGA/DAC with M=10 bits for the application of N=5 phase interpolation. Fig.4 shows that when the maximum amplitude variation is restricted to 1.5dB, the maximum |IPE| value is about 0.7º, which is much smaller than half the phase step, 5.625º. It is important to note that the actual IPE and DPE also depend on the VGA gain accuracy in reality. This issue will be emphasized by the proposed linear digital VGA circuit with associated layout considerations in next section.

III. PHASE ROTATOR CIRCUIT TOPOLOGY

The block diagram of the 10-bit Cartesian phase rotator is shown in Fig. 5. I and Q signals are fed into two 5-bit VGAs whose output currents are summed up to form the interpolated signal, which is further amplified by a high gain buffer.

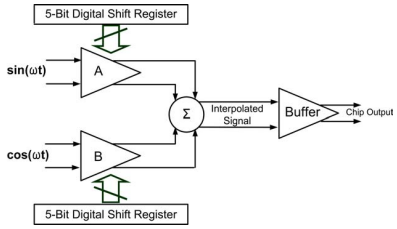

Fig. 5. Block Diagram of Cartesian Phase Rotator

A.. Novel Linear Digital Variable Gain Amplifier

The 5-bit variable gain amplifier is composed of 5 replicas of 1-bit phase rotator cells scaled with binary weights (Fig.6). Every 1-bit phase rotator, effectively a polarity selector, is implemented in a current commutating topology. Fig.7 shows the circuit level details of the Bit0 cell.

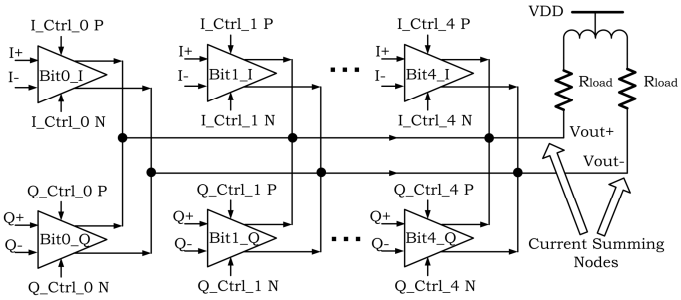

Fig. 6. Block Diagram of Linear Digital Variable Gain Amplifier

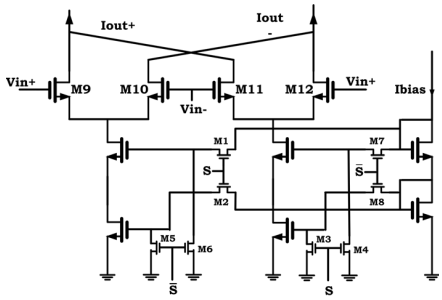

Fig. 7. Circuit Topology of the 1 bit phase rotator (Bit0)

NMOS switches M1-M4 and M5-M8 are controlled by differential logic S & $\overline{S}$ respectively. When S=HIGH ($\overline{S}$=LOW), the left differential pair (M9 & M10) is turned on. This output differential current is normalized to be +1. The right branch is enabled by S=LOW ($\overline{S}$=HIGH) which generates reversed output current with a weight of -1. Complementary logic ensures that only one of the two branches is turned on. This topology draws a constant bias current through the resistive load and maintains a fixed output DC voltage. From an AC perspective, both the input and the

output nodes are loaded by one "on" and one "off" differential pair, which guarantees unchanged parasitic capacitive loadings for a bit-setting-independent frequency response.

To achieve exact 2:1 matching, the bias current and device size in Bit1 is twice that in Bit0. Hence, this Bit1 cell will provide output currents with a weight of +2/-2 determined by the digital controls. The Bit2 cell, which provides AC output currents of +4/-4, also scales in 2:1 fashion with respect to the Bit1 cell, while the Bit3 is realized by combining two Bit2 cells in parallel to avoid any differential nonlinearity matching issues on output AC currents weighting.

Ideally, if the threshold voltages are equal for the corresponding scaling devices mentioned above, their V_{GS} and V_{DS} will also be identical since device width and currents are scaled together. This ensures exact binary-scaled trans-conductances for those bit cells. During implementation, good matching is achieved through optimized layout to reduce stress effect, threshold voltage variation, and process gradient effect. It is noteworthy that this scaling method is independent of transistor modeling, and thus robust to modeling inaccuracy and PVT variations.

Therefore, with the above 4 bits, the VGA achieves normalized AC output currents for all the odd integers within range of -15 to +15 (2).

$$Normalized\ Output\ AC\ Currents = \pm 1 \pm 2 \pm 4 \pm 8 \qquad (2)$$

To achieve even values of the current weight, especially zero, Bit4 is added as the same weight of Bit0 but is controlled only by $\overline{S}$ with its S terminal always grounded. This Bit4 produces a normalized weight of -1 or 0 for $\overline{S}$=HIGH or LOW correspondingly. So the 5-bit VGA normalized gain can be set to any integer between -15 to +15 (3). The weight of -16 is not used to keep symmetry between positive and negative weights.

$$Normalized\ Output\ AC\ Currents = \pm 1 \pm 2 \pm 4 \pm 8 + X \quad (X = 0\ or\ -1) \qquad (3)$$

In order to ensure adequate VGA bandwidth, a peaking inductor is added to the load.

B. Differential High Gain Buffer

Since the VGA is designed to have 0dB voltage gain in order to maximize its bandwidth, an additional 8dB of voltage gain is provided by a two stage differential buffer. The buffer shown in Fig.8 consists of a source follower and a self-biased cascoded differential amplifier to alleviate Miller effect. Inductive peaking is also used for bandwidth extension.

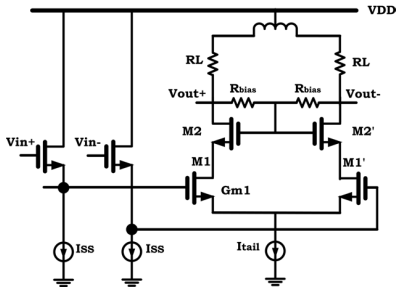

Fig. 8. Circuit Topology of Output Buffer

IV. EXPERIMENT RESULTS

Two phase rotators and their buffers are implemented using the IBM 8RF 0.13um CMOS process. Quadrature signal generation circuitry is not included on this chip, since adjustable input mismatches are needed to show the calibration functionality. Each phase rotator draws 4.8mA from a 2.5V supply, while its buffer consumes 12mA. Fig.9 shows the die photograph. The core area for one phase rotator is 180um × 250um and its peaking inductor occupies 250um × 250um. The total die area is 1.1mm × 1.9mm and is limited by digital pads placed for backup digital control.

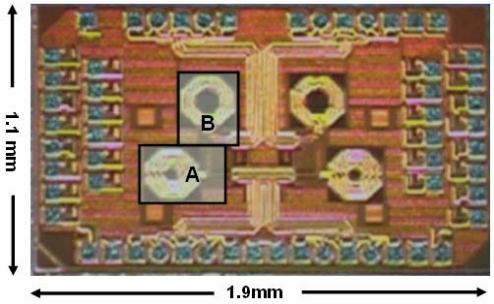

Fig. 9. Die Photograph of the Phase Rotator Chip
Block A is one phase rotator and Block B is its buffer.

A printed circuit board (PCB) measurement setup with Rogers Duriod® 6010 laminates has been designed to characterize the system performance. The chip is mounted using silver epoxy to ensure good backside electrical contact.

A. Phase Shifting Performance

The time domain phase shift testing setup is shown in Fig.10. Differential quadrature signals are generated by a frequency synthesizer with 90º and 180º hybrids. Off-chip phase shifters calibrate input I/Q mismatches at every testing frequency. Digital control signals sweep the output phase of one phase rotator across 360º with an 11.25º step, while the other phase rotator is set at a constant output phase as the reference. Two phase rotator outputs are measured simultaneously by a 4 channel digital oscilloscope.

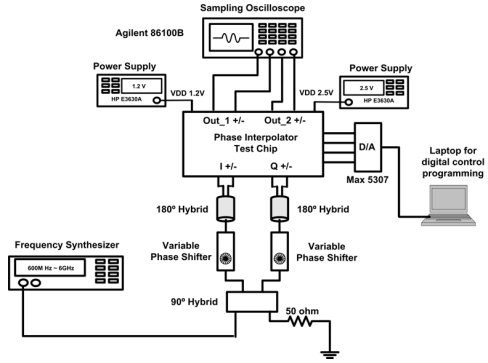

Fig. 10. Measurement Setup for Time Domain Phase Shifting

Fig.11 and Fig.12 show the IPE and DPE results, respectively for 1GHz, 3GHz, and 6GHz measurements with a maximum amplitude variation of 1.5dB. A maximum phase error of about 2º has been achieved for all the frequencies.

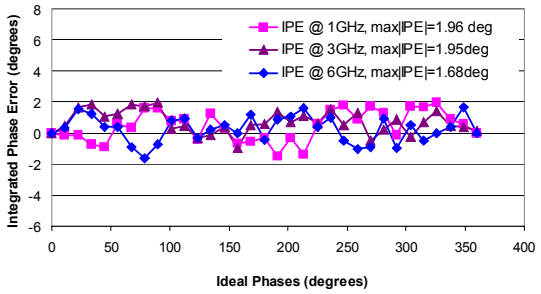

Fig. 11. Integrated Phase Error

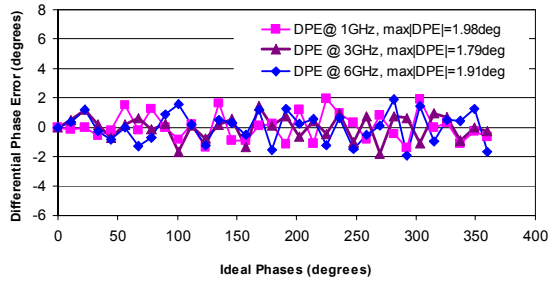

Fig. 12. Differential Phase Error

B. Frequency Response

Coplanar probing is used for S-parameter measurement. The extracted voltage gain is shown in Fig. 13. At low frequency, the gain is 7.8dB while the -3dB bandwidth is around 7.6GHz.

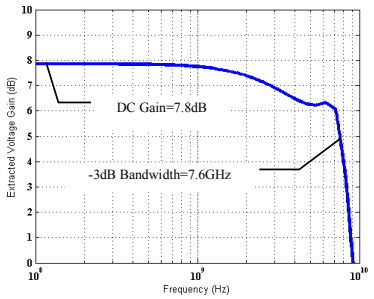

Fig. 13. Extracted Voltage Gain

C. I and Q Mismatch Compensation

As mentioned in Section II, a high resolution Cartesian phase rotator enables compensation for non-ideal quadrature inputs. In this experiment, off-chip phase shifters and attenuators set the 6GHz I/Q inputs with mismatches described as follows.

$$|I| = 1.25 \times |Q| \quad \text{and} \quad \angle Q = \angle I + 100^\circ \qquad (4)$$

Calibration is achieved by sweeping all the interpolated points on the constellation within 3dB amplitude variation and choosing the best matched phases with respect to the ideal phases. Measured IPEs before and after calibration are plotted in Fig.14. The proposed 10-bit phase rotator compensates the mismatched inputs and produces new phase shiftings with a max |IPE| of 1.89º.

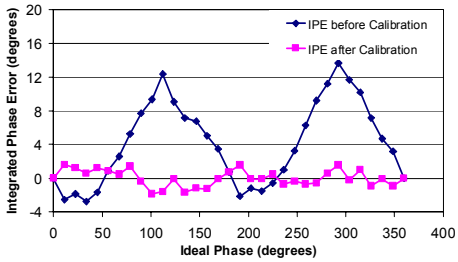

Fig. 14. Calibration for Input I & Q mismatch

V. CONCLUSION

In this paper, a 10-bit wideband phase rotator has been presented. A novel linear digital VGA topology is proposed which is robust to modeling uncertainties and PVT variations. Moreover, this VGA design is highly scalable. The chip layout has been optimized for matching. Together with the buffer, the phase rotator provides 7.8dB of voltage gain and a -3dB bandwidth of 7.6GHz. Accurate phase shifting performance is demonstrated with a maximum phase error of 2º for 32 equal-step phase shifting. Compensation capability on input I/Q mismatch has been shown with measurement results. This significantly relaxes the design of the quadrature signal generation circuit and effectively extends the beam forming system's functioning bandwidth.

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