A Noise-Shifting Differential Colpitts VCO

Roberto Aparicio, *Student Member, IEEE,* and Ali Hajimiri, *Member, IEEE*

***Abstract*—A novel noise-shifting differential Colpitts VCO is presented. It uses current switching to lower phase noise by cyclostationary noise alignment and improve the start-up condition. A design strategy is also devised to enhance the phase noise performance of quadrature coupled oscillators. Two integrated VCOs are presented as design examples.**

***Index Terms*—Analog integrated circuits, CMOS integrated circuits, LC oscillators, optimization, phase noise, quadrature oscillators, radio frequency, voltage-controlled oscillators.**

I. Introduction

INTEGRATED voltage-controlled oscillators (VCOs) are important building elements in the implementation of a single-chip radio in today's communication systems. The ever-growing demand for higher numbers of channels keeps imposing tighter phase noise performance specifications for local oscillators.

Recently, many approaches have been taken to improve the performance of integrated VCOs [1]–[5]. Cross-coupled oscillators have been preferred over other topologies due to their ease of implementation, relaxed start-up condition and differential operation. However, in cross-coupled oscillators, the noise generation by the active devices occurs when the oscillator is quite sensitive to perturbations [6], degrading the phase noise considerably. On the other hand, the Colpitts oscillator [7] has superior cyclostationary noise properties and can hence potentially achieve lower phase noise [8]. Despite these advantages, single-ended Colpitts oscillators are rarely used in today's integrated circuits due to their higher required gain for reliable start-up and single-ended nature that makes them more sensitive to parameter variations and common-mode noise sources, such as substrate and supply noise. Moreover, quadrature signals are typically required in many receiver and transmitter architectures [9], where the accuracy of such quadrature signals would determine the image rejection [10], [11]. A differential quadrature oscillator is thus preferred over a single-ended one.

This paper presents a new oscillator topology that overcomes these issues. It improves the phase noise performance by cyclostationary noise alignment while providing a fully differential output and a large loop gain for reliable start-up. It is also shown that, via optimum coupling of two cross-coupled oscillators, quadrature outputs can be obtained with an enhanced phase noise performance.

Manuscript received April 30, 2002; revised July 1, 2002. This work was supported in part by the Lee center for advance networking, NSF-ERC, ONR-MURI, and a fellowship from IBM Corporation.

The authors are with the California Institute of Technology, Pasadena, CA 91125 USA (e-mail: aparicio@caltech.edu).

Digital Object Identifier 10.1109/JSSC.2002.804354

Section II reviews the noise generation and conversion mechanics. Section III compares the existing oscillator topologies with an emphasis on the cyclostationarity of noise sources. Section IV presents the design evolution leading to the topology presented in this paper. Section V describes a strategy to optimally couple two oscillators for quadrature signal generation with enhanced phase noise performance. Finally, Section VI presents the experimental results from two different oscillators as design examples.

II. Noise Generation Mechanisms

In an oscillator, the total single-sideband phase noise in the $1/f^2$ region of the spectrum is given by [6]

$$L\{\Delta\omega\} = \frac{\bar{i_n^2}/\Delta f}{2q_{\max}^2} \cdot \frac{\Gamma_{\text{eff,rms}}^2}{\Delta\omega^2} \tag{1}$$

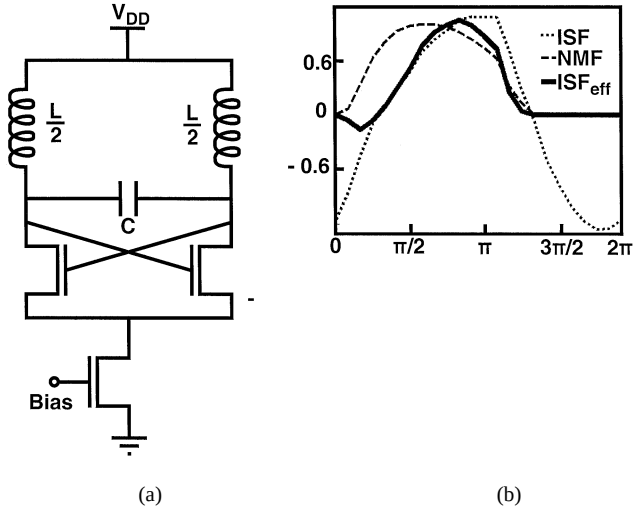
where $\Delta\omega$ is the offset frequency from the carrier, $\bar{i_n^2}/\Delta f$ is the power spectral density of the current noise source in question, $\Gamma_{\text{eff,rms}}$ is the rms value of the effective impulse sensitivity function (ISF) associated with that noise source, and $q_{\max}$ is the maximum charge swing across the current noise source. The effective ISF is the product of the ISF and the noise-modulating function (NMF), as defined in [6], i.e.

$$\Gamma_{eff}(\omega t) = \Gamma(\omega t) \cdot \alpha(\omega t) \tag{2}$$

where the ISF, denoted as $\Gamma(\omega t)$, represents the time-varying sensitivity of the oscillator's phase to perturbations and the NMF, shown as $\alpha(\omega t)$, describes the modulation of the noise power spectrum with time for the noise source in question.

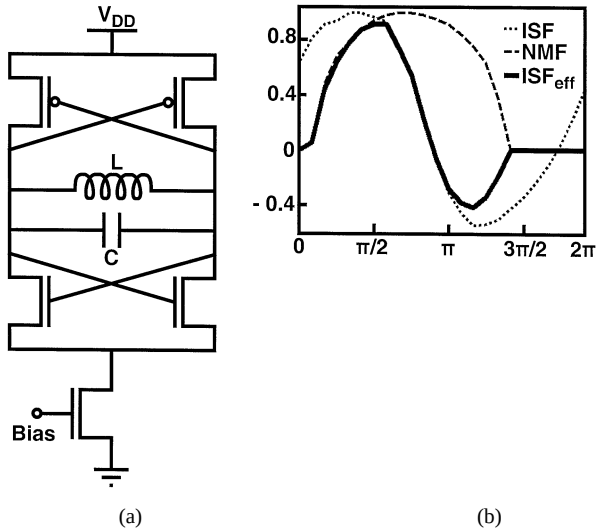
In practice, an active device creates an energy restoring mechanism to compensate for the losses of the tank and thus sustain the oscillation. This device acts as a means to transfer the energy from the dc power supply to the resonant tank. Unfortunately, during this energy transfer process, the active device injects noise into the tank, which in turn becomes phase noise. In essence, (1) states quantitatively the way the phase noise is affected by these processes [12].

Equation (1) indicates that an oscillator should have a $q_{\max}$ as high as possible with a $\Gamma_{\text{eff,rms}}$ as small as possible to lower the phase noise. To increase $q_{\max}$ in an oscillator, the ratio of the tank energy to the dc power dissipation should be maximized [12]. On the other hand, $\Gamma_{\text{eff,rms}}$ strongly depends on the shape of Γ_{eff}, which in turn has a close relation with the timing of the energy injection into the tank. In this context, it is highly desirable that the energy should be delivered all at once at the minimum sensitivity point, as discussed in detail in [8].



(a) (b)

Fig. 1. NMOS-only cross-coupled oscillator. (a) Circuit schematic. (b) ISF, NMF, and effective ISF waveforms.



(a) (b)

Fig. 2. Complementary cross-coupled oscillator. (a) Circuit schematic. (b) ISF, NMF, and effective ISF waveforms.

III. Oscillator Topology Comparison

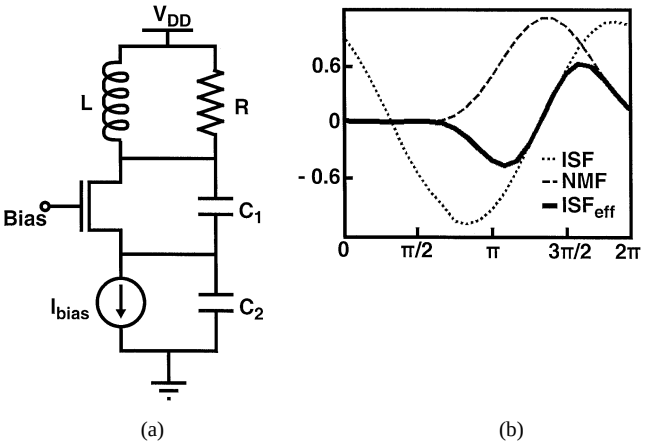
In this section, several oscillator topologies will be compared with an emphasis on their cyclostationary noise properties and energy transfer efficiencies to obtain essential understanding of their effect on the oscillator's phase noise performance.

Fig. 1(a) shows the NMOS-only cross-coupled oscillator topology, widely used in high-frequency integrated circuits due to the ease of implementation and differential operation. Fig. 2(a) shows the complementary version using both NMOS and PMOS transistors. This topology provides a larger tank amplitude for a given tail current in the current limited regime defined in [8]. Finally, Fig. 3(a) depicts the single-ended Colpitts oscillator topology, which is a commonly used single-ended design [2], [7].

To simulate the ISF and NMF waveforms of the above mentioned oscillators, the *direct impulse response measurement* method of [6] is implemented in HSpice [13]. The three oscillators are simulated using the same tank inductance and are tuned to oscillate at a center frequency of 1.8 GHz, while maintaining a tuning range of at least 20%. The inductors have a quality factor of 5 at 1.8 GHz. Finally, the oscillators draw the same bias current and operate in the current limited regime.

Fig. 1(b) shows the simulated $\Gamma(\omega t)$, $\alpha(\omega t)$ and $\Gamma_{\rm eff}(\omega t)$ waveforms of the NMOS transistor channel noise in the NMOS-only cross-coupled topology of Fig. 1(a). In this oscillator, the maximum noise generated by the active devices appears when the oscillator is quite sensitive to perturbations. This can be noticed in Fig. 1(b), where the maximums of the NMF and ISF almost overlap, resulting in a large effective ISF and thus worsening the phase noise for a given resonator quality factor and bias current.

Fig. 2(b) shows the simulated waveforms for the PMOS transistors in the complementary cross-coupled oscillator of Fig. 2(a). The waveforms of the NMOS transistors are comparable and are omitted without loss of generality. Similar to the NMOS-only cross-coupled topology discussed previously, the noise generated by the active devices of the complementary cross-coupled oscillator of Fig. 2(a) is maximum when the oscillator's phase is quite sensitive to perturbations. Moreover, in this topology the noise generated by both PMOS and NMOS transistors add to the overall active noise of the oscillator. Nevertheless, the complementary cross-coupled oscillator shows a better phase noise performance when compared to the NMOS- or PMOS-only cross-coupled oscillators for the same supply voltage and bias current when operating at the current limited regime, as demonstrated experimentally in [14]. This is mainly because the complementary cross-coupled oscillator of Fig. 2(a) presents a larger maximum charge swing $q_{\rm max}$ than that of the NMOS- or PMOS-only cross-coupled oscillators which overall enhances its phase noise performance, as will be discussed shortly.



(a) (b)

Fig. 3. Single-ended Colpitts oscillator topology. (a) Circuit schematic. (b) ISF, NMF, and effective ISF waveforms.

It is instructive to compare the contributions of each of the noise sources to the total phase noise in the complementary cross-coupled topology Fig. 2(a). Table I shows the simulated phase noise contributions of different noise sources at 600-kHz offset from a 1.8-GHz carrier of the cross-coupled oscillator depicted in Fig. 2(a). It can be clearly seen that most of the circuit noise is generated by the drain current noise of the cross-connected transistors, while the combined contributions of the other

TABLE I
PHASE NOISE CONTRIBUTION OF EACH NOISE SOURCE

Noise Source	Contribution
Drain current	87%
Inductor	6%
Tail Current	5%
Varactor	2%

noise sources accounts for less than 13% of the total phase noise power. For instance, if the noise injected by the tail device could be completely removed, the total phase noise would only show an improvement of 0.22 dB in this oscillator example.

On the other hand, the single-ended Colpitts oscillator of Fig. 3(a) has better cyclostationary noise properties, as exhibited in the simulated $\Gamma(\omega t)$, $\alpha(\omega t)$, and $\Gamma_{\rm eff}(\omega t)$ waveforms depicted in Fig. 3(b). In this topology, the maximum noise generation instant is aligned with the oscillator's minimum sensitivity point and can hence potentially achieve lower phase noise. Also, the Colpitts oscillator presents a smaller rms and dc value of its effective ISF than that of the NMOS- or PMOS-only and complementary cross-coupled oscillators of Figs. 1(a) and 2(a), respectively. A more symmetrical effective ISF will significantly reduce the up-conversion of the low-frequency noise of the transistor [6].

As previously discussed, while the better cyclostationary properties of an oscillator alone would enhance the phase noise performance, a large oscillation charge swing results in an improved tank energy. The tank energy $E_{\rm tank}$ in an oscillator is given by $E_{\rm tank} = CV_{\rm tank}^2/2$, where $V_{\rm tank}$ is the tank voltage amplitude. Moreover, if the oscillator operates in the current limited regime, $V_{\rm tank}$ can be expressed in terms of the bias current $I_{\rm bias}$ and the effective parallel tank resistance $R_{\rm tank}$, i.e.

$$V_{\rm tank} = \beta R_{\rm tank} I_{\rm bias} \tag{3}$$

where β is the oscillation amplitude constant. The energy transfer efficiency η, which is defined as the ratio of the energy stored in the resonator's tank $E_{\rm tank}$ to the total dc energy $P_{\rm dc}$ dissipated in one period, can be expressed as

$$\eta = \frac{E_{\rm tank}}{P_{\rm dc}T} = \frac{CV_{\rm tank}^2 f_{\rm osc}}{2V_{\rm dc}I_{\rm bias}} = \frac{Q_{\rm tank}^2 \beta^2 I_{\rm bias}}{4\pi V_{\rm dc}} \cdot \sqrt{\frac{L}{C}} \tag{4}$$

where $T = 1/f_{\rm osc} = 2\pi\sqrt{LC}$ is the oscillation period and $V_{\rm dc}$ is the supply voltage. Also, it is assumed that the quality factor of the tank is given by $Q = R_{\rm tank}/(2\pi f_{\rm osc} L)$.

Equation (4) shows the well-known fact that increasing the tank's quality factor will improve the energy transfer efficiency and enhance the phase noise of the oscillator. However, this energy transfer efficiency can also be increased if the oscillator has a larger oscillation amplitude for a given bias current (i.e., larger β). To illustrate this, Table II compares the oscillation amplitude constant β for the NMOS- and PMOS-only, complementary cross-coupled and Colpitts VCOs of Figs. 1(a), 2(a), and 3(a), respectively. It can be easily seen that the Colpitts oscillator presents a higher output voltage swing and higher energy transfer efficiency than that of the NMOS- or PMOS-only and complementary cross-coupled oscillators for a given bias current, which will further enhance its phase noise. It is also noteworthy that the effieciency is proportional only to the square root of the L/C ratio. Interestingly, in the case of integrated spiral inductors, reducing the L results in a stronger improvement in the Q^2 term compared to the $\sqrt{L/C}$, as discussed in more detail in [12].

TABLE II
OSCILLATION COMPARISON

Oscillator	Amplitude	Oscillation amplitude constant β	Energy transfer efficiency η
NMOS- or PMOS-only cross-coupled	$\frac{2}{\pi}R_{tank}I_{bias}$	$2/\pi$	$\frac{Q_{tank}^2 I_{bias}\sqrt{L/C}}{\pi^3 V_{dc}}$
Complementary cross-coupled	$\frac{4}{\pi}R_{tank}I_{bias}$	$4/\pi$	$\frac{4Q_{tank}^2 I_{bias}\sqrt{L/C}}{\pi^3 V_{dc}}$
Single-ended Colpitts	$2R_{tank}I_{bias}$	2	$\frac{Q_{tank}^2 I_{bias}\sqrt{L/C}}{\pi V_{dc}}$

Despite these advantages, single-ended Colpitts oscillators are rarely used in today's integrated circuits, due to the higher required gain for reliable start-up and their single-ended nature that makes them more sensitive to common-mode noise sources such as substrate and supply noise. In the following section, we will present a new topology that remedies these problems. Most of the discussed properties of the single-ended Colpitts oscillator of Fig. 3(a) are applicable to the oscillator topology presented next.

IV. NOISE-SHIFTING COLPITTS OSCILLATOR

In this section, starting from the single-ended Colpitts oscillator of Fig. 3(a), we will show the design evolution that leads to a topology that overcomes the start-up issues while providing a low-noise fully differential output.

A differential output can be provided by coupling two identical Colpitts oscillators and sharing their source-to-ground capacitors C_2, as shown on Fig. 4(a). Since the center node where both C_2 capacitors are connected together is a differential virtual ground, the original operation of the oscillators remains unchanged when the two sides oscillate 180° out of phase. The differential operation will be guaranteed if the center node is left floating and is not grounded. Fig. 4(b) shows the simulated voltage and current waveforms of this topology.

This differential topology is insensitive to any extra parasitic inductance and capacitance due to the metal lines and wire bonds used to provide the ground and supply voltage to the oscillator. On the other hand, this topology increases the power consumption by a factor of two, if the same start-up condition is to be met. Nevertheless, the power transfer efficiency remains constant, as the output voltage swing of this differential topology is twice but the overall capacitance is half than that of the single-ended Colpitts oscillator of Fig. 3(a).

Noting that the current through the main transistor in each of the Colpitts oscillators of Fig. 4(a) flow for less than half of the oscillation period, as shown in Fig. 4(b). It is therefore possible and favorable to replace the source-to-ground dc current source

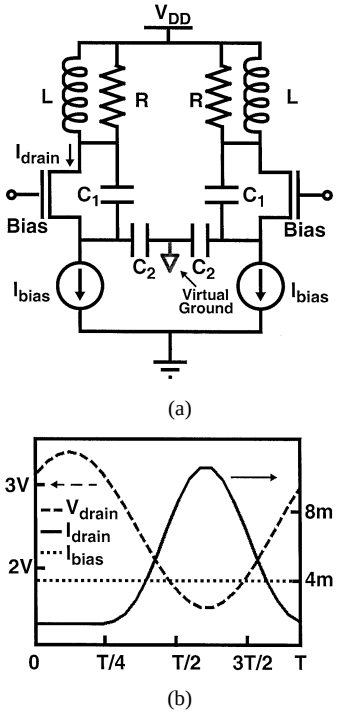


Fig. 4. Differential Colpitts oscillator. (a) Circuit topology. (b) Simulated voltage and current waveforms.

by the same dc current source and a timed switch which alternates the current between the two sides of the oscillator at the frequency of oscillation, as shown in Fig. 5(a).

The switching has to occur in a synchronized manner and can be achieved by using a pair of NMOS transistors to switch the current from one side to the other, as shown in Fig. 5(b). Moreover, the negative resistance of this tail cross-coupled pair provides a very effective means to enhance the small-signal loop gain, improving the start-up condition.

Finally, to add frequency tuning capabilities to the proposed oscillator topology, it is possible to include two varactors connected in parallel with the tank inductor. Also, the two shared C_2 capacitors connected in series can be replaced by an equivalent capacitor with half the value. The final oscillator topology is shown in Fig. 6(a) and the simulated ISF, NMF, effective ISF, and voltage waveforms for the core transistor are depicted in Fig. 6(b). In this configuration, the transistor channel noise is maximum when the oscillator is the least sensitive to perturbations, reducing the effective ISF considerably. Therefore, this topology takes full advantage of the cyclostationary noise shaping of the core transistors. The NMOS cross-coupled transistors of Fig. 6(a) operate mostly between ohmic and cut-off regions and hence have smaller noise contribution. Moreover, this noise contribution is attenuated by the capacitive voltage divider formed by C_1 and C_2. This voltage divider has the primarily function to provide a positive feedback path and enhance the small-signal loop gain of the oscillator.

V. Quadrature Generation

Quadrature components of a VCO output are needed in most receivers and transmitters for vector modulation and demodulation [15] and image rejection [9]–[11]. The phase and amplitude accuracy of these outputs is critical to the performance of such systems. There are several options for on-chip quadrature signal generation.

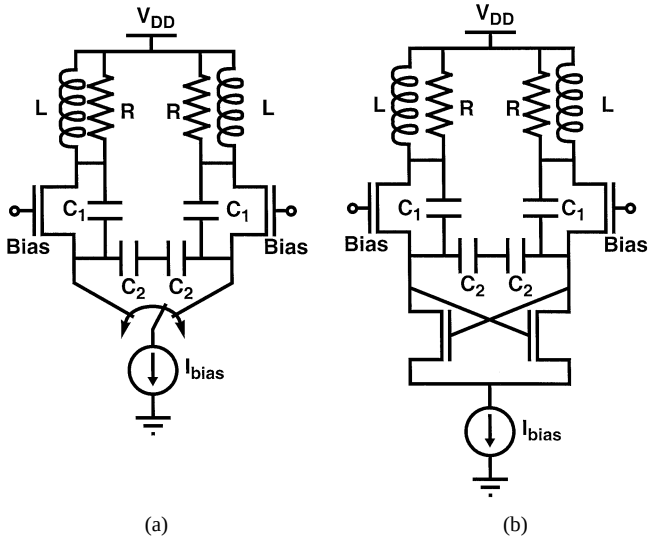


Fig. 5. Current switching topology evolution. (a) Timed switch implementation. (b) NMOS transistors implementation.

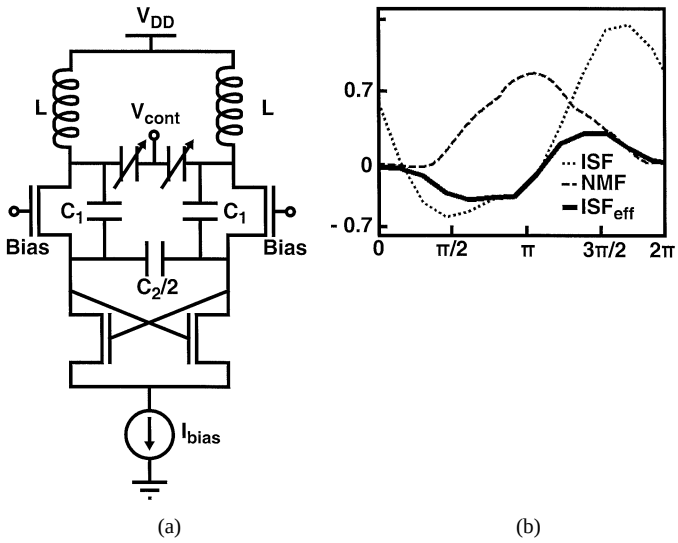


Fig. 6. Noise shifting differential Colpitts VCO. (a) Final topology. (b) ISF, NMF, and effective ISF waveforms for the core transistor.

In the first approach, the output of the VCO is applied to a polyphase filter. A polyphase filter is an RC-CR network that in the ideal case shifts its outputs by $\pm 90^{\circ}$ with respect to one another. Unfortunately, this phase shift occurs only in a narrow frequency range and the accuracy of the in-phase and quadrature signals is strongly dependent on the on-chip component matching. Although cascading several stages of stagger-tuned polyphase filters can alleviate this problem [16], unwanted additonal loss is added, requiring amplifiers/buffers to compensate for loss of the filter, at the extra penalty of higher power consumption. On the other hand, if the polyphase filter is directly connected in parallel with the oscillator tank, the loading of the tank will lower the signal amplitude and increase the noise. Also, a larger area and better matching are required while

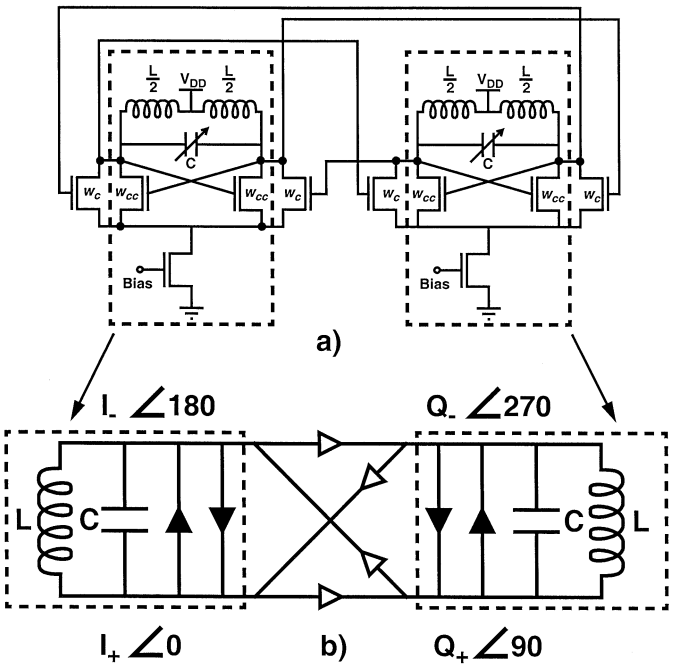


Fig. 7. Quadrature-coupled *LC* VCO. (a) Circuit topology. (b) Block diagram.

the phase noise is degraded due to the extra sources of loss and noise.

The second option is the combination of a VCO operating at twice the frequency of interest and a divide-by-two circuit. If a master–slave flip flop is used, the power consumption is considerably increased. Also, in a master–slave flip-flop, any asymmetry in the duty cycle of the input or mismatch at the input of the divider can result in a significant degradation in the quadrature accuracy. Methods such as level-locked loops (LLLs) [17] have been proposed to solve this problem, but they increase the power consumption.

The third option is to couple two identical oscillators in such a way that forces their outputs to oscillate 90° out of phase. Fig. 7(a) shows the typical approach to practically couple two NMOS-only cross-coupled oscillators [18]. This configuration has the disadvantage of requiring twice the area and power than that of a single *LC* oscillator. However, it is not clear if this solution outperforms the previous ones with regards to phase noise and quadrature accuracy.

To help us understand how this coupling works, Fig. 7(b) depicts the block diagram of the circuit shown in Fig. 7(a). The four output nodes, namely I_+, Q_+, I_-, and Q_-, have the same amplitude and frequency but are shifted 90° out of phase, respectively. The solid triangles signify the cross-coupled pair of NMOS transistors, while the hollow triangles denote the coupling transistors between the two oscillators. Under normal operation conditions, the cross-coupled transistors operate fully switching and provide 180° phase shift from input to output [solid triangles, Fig. 7(b)]. Due to the symmetry of the circuit configuration and as the oscillator would oscillate in the state of equilibrium, the coupling transistors [hollow triangles, Fig. 7(b)] operate providing a 90° phase shift between the input to output. In other words, for instance, if one assumes that the oscillator on the left-hand side is $90° + \Delta$ ahead of the one on the right, one can argue that looking at the mirror image of the oscillator we will see that the left-hand side is $90° - \Delta$ ahead. Assuming that both sides are identical, we should have $90° + \Delta = 90° - \Delta$ and thus $\Delta = 0$.

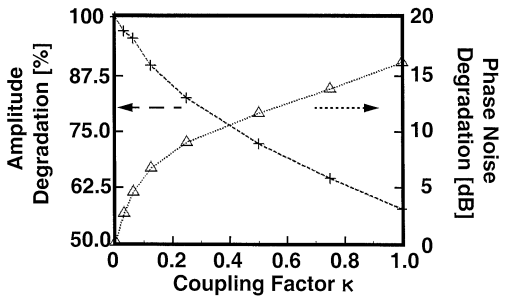


Fig. 8. Amplitude and phase noise degradation versus the coupling factor.

To evaluate the effect of the extra loading of the coupling transistors on the amplitude of the quadrature *LC* oscillator, the circuit topology of Fig. 7(a) is simulated. For this set of simulations, the VCO is designed to oscillate at 1.8 GHz while having more than 20% of frequency tuning and operating at the current limited regime. The inductors have a quality factor of 5. The coupling factor κ is defined as the ratio of the width of the coupling transistor w_c to the width of the cross-connected transistor w_{cc}, i.e., $\kappa = w_c/w_{cc}$. If the sizes of the coupling transistors are on the same order of magnitude than the cross-coupling transistors, their effective g_m would load the tank significantly, reducing the output voltage swing and thus worsening the phase noise. The simulation results showing the amplitude degradation versus the coupling factor κ are depicted in Fig. 8 by the dashed line. Amplitude degradation can be defined as the ratio of the amplitude of the quadrature *LC* oscillator of Fig. 7(a) to that of the same oscillator when there is no coupling, i.e., $\kappa = 0$. As can be seen, the oscillation amplitude decreases for larger coupling ratios. For instance, the oscillation amplitude is degraded by more than 40% for $\kappa = 1$. The phase noise degradation of the oscillator versus κ is also depicted in Fig. 8 by a dotted line. Phase noise degradation is defined as the excess of phase noise when compared to the oscillator with no coupling, i.e., $\kappa = 0$. For this example, the simulated phase noise is measured at 600-kHz offset from a 1.8-GHz carrier. As expected, the phase noise is degraded for higher coupling ratios by as much as 16 dB for $\kappa = 1$. It is noteworthy that not only the amplitude reduction of the quadrature *LC* oscillator of Fig. 7(a) contributes to the worse phase noise performance for larger coupling ratios, but also the coupling transistors generate noise in proportion to the coupling factor κ. This noise in turn becomes phase noise and accounts for the extra degradation on the phase noise for larger κ. The amount of amplitude and phase noise degradation for a given quadrature *LC* oscillator and a given κ will depend on the effective loading of the coupling transistors to the oscillator tank.

To evaluate the effect of component mismatch on the phase and amplitude accuracy of the quadrature *LC* oscillator of Fig. 7(a), a tank referred capacitor is inserted between one of the output nodes of the oscillator and ground. This capacitor is introduced to imitate any unbalanced loading produced by the following stages of the oscillator, such as buffers/amplifiers

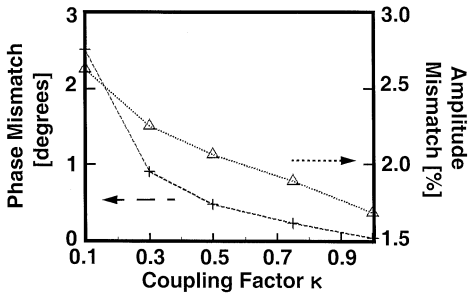


Fig. 9. Amplitude and phase mismatch versus the coupling factor for a tank referred capacitor of 2%.

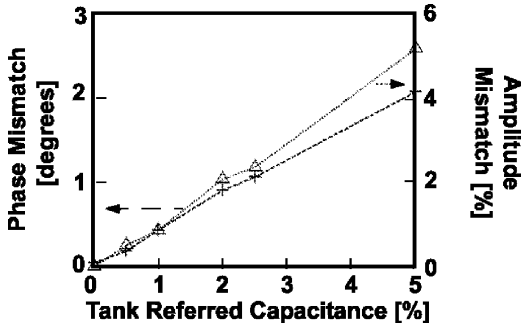


Fig. 10. Amplitude and phase mismatch versus the tank referred capacitor for $\kappa = 0.3$.

and mixers, or by any asymmetry in the layout. The capacitance value of the tank referred capacitor corresponds to that of the tank capacitance expressed in percentage. Thus, a tank referred capacitor of 5% corresponds to an extra loading capacitor whose value is 0.05 that of the tank capacitance. For the second set of simulations, a tank referred capacitor of 2% is added to one of the outputs of the quadrature *LC* oscillator of Fig. 7(a). The simulation results showing the phase and amplitude mismatch versus the coupling factor κ for the quadrature oscillator of Fig. 7(a) are depicted in Fig. 9 by dashed and dotted lines, respectively. It can easily be seen that the phase and amplitude accuracy of the quadrature outputs is compromised for smaller coupling factors and this degradation is inversely proportional to κ. To visualize this tradeoff further, Fig. 10 depicts the simulation results showing the phase and amplitude mismatch for different values of a tank referred capacitor for the oscillator of Fig. 7(a) with a coupling factor of $\kappa = 0.3$ by dashed and dotted lines, respectively. As expected, the phase and amplitude accuracy of the quadrature *LC* oscillator of Fig. 7(a) is degraded for a larger capacitance inbalance. However, it is noteworthy that, for a tank referred capacitor as high as 2% of the tank capacitance, the phase mismatch is smaller than 1° and the amplitude mismatch is less than 2.5%, as shown in Fig. 10.

Quadrature *LC* oscillators also suffer from mismatches of other components due to process variations such as transistor gain and tank inductance value. However, due to the nonlinear behavior and gain compression mechanisms of the oscillator, the cross-coupled transistor mismatch has a smaller affect on the accuracy of the quadrature signals. Also, uncertainties in the inductance value can be small, as the value is determined by lithographic processes which are quite accurate in today's process technologies.

Based on these arguments, a design strategy can be summarized for improving the amplitude and phase accuracy for the quadrature *LC* oscillator of Fig. 7 in the following way.

1) Find the maximum tank capacitance that satisfies the oscillator design specifications, such as frequency tuning, tank amplitude, and start up. This will decrease the effect of capacitive mismatch on the amplitude and phase accuracy of the quadrature signals.
2) Compensate for any asymmetric loading on the nodes of the quadrature oscillator. Try to lay out the oscillator with a high degree of symmetry while balancing any extra interconnecting capacitance. Also, equalize the length and the differential capacitance of the connecting metal lines of the quadrature *LC* oscillator.

If the phase noise performance is of primary concern, decrease the ratio of the coupling transistors. However, this will increase the amplitude and phase mismatch of the quadrature outputs limiting its practical use to compensating any unbalanced capacitances.

Although the arguments presented in this section were limited to the coupling of the NMOS-only cross-coupled VCO of Fig. 1(a), they are equally applicable to the complementary cross-coupled oscillator of Fig. 2(a) and the differential noise-shifting Colpitts oscillator of Fig. 6(a) using similar lines of argument.

It is noteworthy that the first design strategy is in good agreement with the optimization presented in [17] for phase noise performance of integrated *LC* VCOs.

VI. Experimental Results

Two test oscillators were fabricated in two different process technologies. The differential noise-shifting Colpitts VCO of Fig. 6(a) was implemented in the first test chip. It was fabricated in a 0.35-μm BiCMOS process technology, using NMOS transistors only. The oscillator is designed for a center frequency of 2.1 GHz. The inductors have quality factors of 6. The NMOS transistors operating in inversion mode are used as varactors. The channel length of the NMOS varactors is optimized to maximize the quality factor while maintaining a good tuning range. Open drain transistors are used as drivers and are designed to drive a 50-Ω load at 0 dBm.

The test VCO is optimized using graphical linear programming [12]. The design constrains are: to maximize the voltage swing while maintaining a loop gain of at least three for reliable start up. The capacitor C_2 is chosen to be four times C_1 for near optimum operation [8].

Fig. 11 shows the die photo of the prototype VCO, where the main blocks of the oscillator are highlighted. Two extra components, namely, an inductor L_t and a capacitor C_t, are also included to evaluate the effect of the tail current noise filtering on the phase noise of the oscillator [14], [19], which will be discussed shortly. These two elements can be trimmed out using a laser.

The oscillator operates from 1.8 to 2.45 GHz, which corresponds to a center frequency of 2.12 GHz and a tuning range

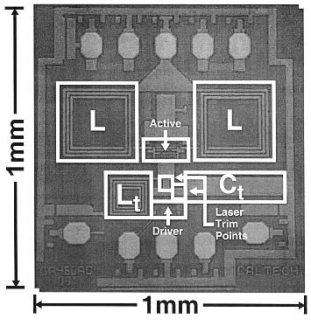


Fig. 11. Differential Colpitts oscillator die micrograph.

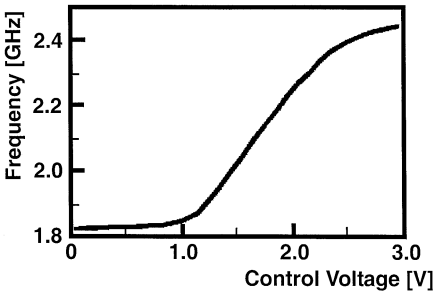


Fig. 12. Differential Colpitts oscillator frequency tuning.

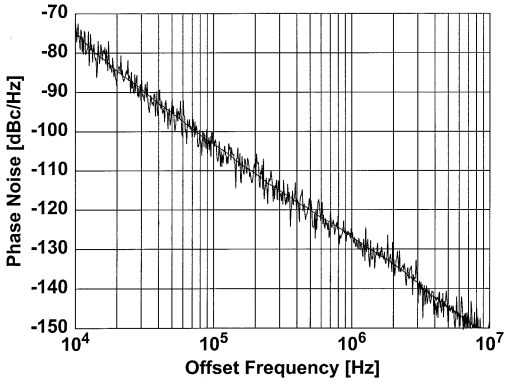


Fig. 13. Measured phase noise vesus offset frequency at 1.8 GHz.

of 30.5%, as shown in Fig. 12. It can be noted that the voltage to frequency transfer function of the VCO is very linear over more than 500 MHz, which corresponds to 80% of the frequency tuning of the VCO. The oscillator phase noise is measured using an NTS-1000 phase noise analyzer as well as an HP8563 spectrum analyzer with phase noise measurement utility. Fig. 13 shows the plot of the phase noise versus the offset frequency from the 1.8-GHz carrier. The oscillator shows a phase noise of -139 dBc/Hz at 3-MHz offset using a low inductor Q of 6, while drawing 4 mA from a 2.5-V supply.

To verify the effect of capacitive [14] and *LC* [19] tail current noise filtering, they were added to the oscillator with the option to remove the inductor or capacitor through a laser trim. The *LC* network was designed to resonate at twice the frequency of oscillation. The measured phase noise of the oscillator at 3-MHz offset from a 1.8-GHz offset carrier was -138.2 dBc/Hz with the *LC* filter and -139.2 dBc/Hz with the capacitor alone and inductor shorted [14].

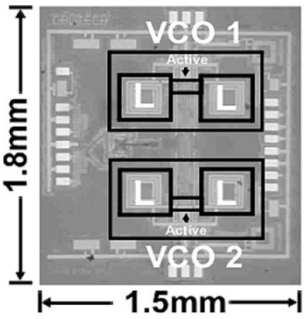


Fig. 14. Quadrature NMOS-only cross-coupled oscillator die photo.

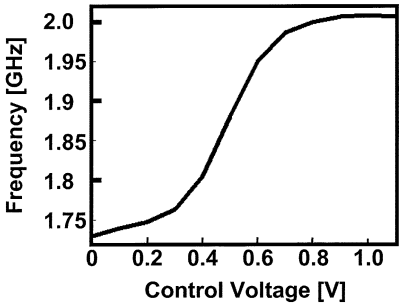


Fig. 15. Quadrature NMOS-only cross-coupled oscillator frequency tuning.

The *LC* filtering method does not have a significant effect on phase noise of the implemented VCO, as the simulated noise component of the tail device contributes to less than 5% of the oscillator's phase noise in the $1/f^2$ region. Therefore, in spite of filtering the noise component from the tail device at twice the oscillation frequency, the L_t inductor acts as a source of wide-band noise, which degrades the overall phase noise by less than 1 dB. Also, the filtering at $2f_o$ cannot be done at the drain of the cross-coupled transistors, as it will filter the switched current as well.

A second test chip implementing the quadrature NMOS-only cross-coupled VCO of Fig. 7(a) was fabricated in a 0.18-μm BiCMOS process technology using the NMOS transistors only. For this design, the oscillator is designed for a center frequency of 1.8 GHz and NMOS transistors operating in inversion mode are used as varactors.

The implemented quadrature *LC* VCO is aimed to evaluate the effect of the relative coupling on the phase noise of the quadrature oscillator. Therefore, very special care is taken to layout the VCO. Also, the design strategies proposed in Section V are carefully followed. Fig. 14 shows the quadrature *LC* VCO test chip photograph.

The quadrature oscillator draws a total of 4 mA of current from a 1-V supply and operates from 1.72 to 2.02 GHz. These correspond to a current consumption of 2 mA per *LC* oscillator, a center frequency of 1.87 GHz, and a tuning range of 16%. The voltage to frequency transfer function of the oscillator is depicted in Fig. 15.

Phase noise is measured using an NTS-1000 phase noise analyzer as well as an HP8563 spectrum analyzer with phase noise measurement utility. The quadrature *LC* oscillator shows a phase noise of -100.7 dBc/Hz at 600-kHz offset from a 1.72-GHz carrier for a coupling factor of $\kappa = 0.35$. To evaluate

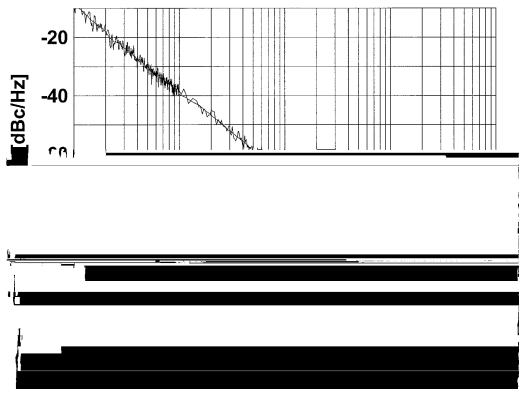


Fig. 16. Measured phase noise versus offset frequency at 1.72 GHz.

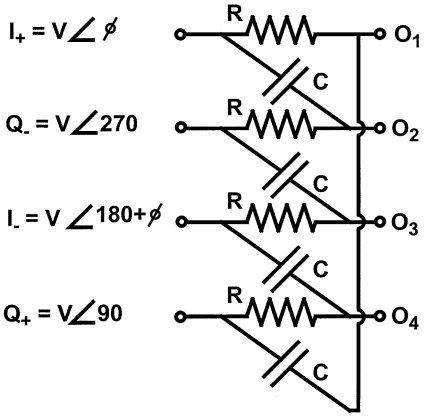


Fig. 17. *RC* polyphase network.

the effect of the relative coupling of the oscillator on its phase noise, the coupling factor can be modified to $\kappa = 0.05$ by means of a laser trim. The measured phase noise for a coupling factor $\kappa = 0.05$ is -113.5 dBc/Hz at 600-kHz offset from a 1.72-GHz carrier. Fig. 16 shows a plot of phase noise versus the offset frequency. It is shown experimentally that the phase noise is enhanced by 12.7 dB by having a smaller coupling factor κ while maintaining the same supply voltage and bias current.

To estimate the phase accuracy of the VCO's quadrature outputs, a polyphase network is also integrated on the same chip. The polyphase schematic and terminal interconnections are shown in Fig. 17. If the inputs to the polyphase are in quadrature and have an amplitude V, but with a phase mismatch of ϕ degrees as depicted in Fig. 17, the magnitude of the difference of the outputs of the polyphase at $2\pi f = 1/(RC)$ can be shown to be

$$|O_1 - O_3| = |O_2 - O_4| = V \cdot 2\sqrt{2}\left|\sin\frac{\phi}{2}\right|. \qquad (5)$$

Therefore, the phase error can be extrapolated by measuring the differential output voltage amplitude of the polyphase. Buffers are required to prevent excessive loading to the polyphase and drive the 50-Ω load of the measurement equipment. Microwave coplanar probes are used to probe the RF output pads of the buffers. An HP 8563E spectrum analyzer is used to measure the output power. Using the simulated values for the buffers gain, the extrapolated phase error ϕ is found to be less than 1° in both cases.

VII. Conclusion

A novel noise-shifting differential Colpitts VCO is presented. It uses current-switching to lower phase noise by cyclostationary noise alignment and improve the start-up. A design strategy is also devised aimed to enhancing the phase noise performance of quadrature *LC* oscillators. The tradeoff between quadrature accuracy and phase noise performance is also shown.

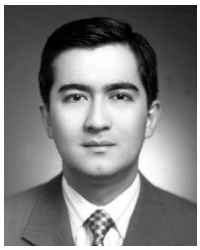
Acknowledgment

The authors would like to thank Skyworks Solutions and Jazz Semiconductor for fabrication of the oscillators and, in particular, S. Lloyd, R. Magoon, F. In'tveld, and B. Bhattacharyya of Skyworks Solutions (formerly known as the Wireless Communication Division of Conexant) and M. Racanelli, S. Stetson, and A. Karroy of Jazz Semiconductor for consistent support and help. They would also like to acknowledge I. Aoki, D. Ham, and S. Kee of the California Institute of Technology for valuable technical discussions.

References

[1] J. Craninckx and M. Steyaert, "A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1474–1482, Dec. 1995.
[2] M. Soyuer, K. A. Jenkins, J. N. Burghartz, and M. D. Hulvey, "A 3-V 4-GHz nMOS voltage-controlled oscillator with integrated resonator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2042–2045, Dec. 1996.
[3] B. Razavi, "A 1.8-GHz CMOS voltage-controlled oscillator," in *ISSCC Dig. Tech. Papers*, 1997, pp. 388–389.
[4] J. Craninckx and M. Steyaert, "A fully integrated CMOS DCS-1800 frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2054–2065, Dec. 1998.
[5] C. Lam and B. Razavi, "A 2.6-GHz/5.2-GHz CMOS voltage-controlled oscillator," in *ISSCC Dig. Tech. Papers*, 1999, pp. 402–403.
[6] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179–194, Feb. 1998.
[7] N. M. Nguyen and R. G. Meyer, "Start-up and frequency stability in high-frequency oscillators," *IEEE J. Solid-State Circuits*, vol. 27, pp. 810–820, May 1992.
[8] A. Hajimiri and T. H. Lee, *The Design of Low Noise Oscillators*. Norwell, MA: Kluwer, 1999.
[9] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers—Theory, design and applications," *IEEE T. Microwave Theory Tech.*, vol. 50, pp. 288–301, Jan. 2002.
[10] J. W. Archer, J. Granlund, and R. E. Mauzy, "A broad-band VHF mixer exhibiting high image rejection over a multidecade baseband frequency range," *IEEE J. Solid-State Circuits*, vol. SC-16, pp. 385–392, Aug. 1981.
[11] J. C. Rudell, J.-J. Ou, T. B. Cho, G. Chien, F. Brianti, J. A. Weldon, and P. R. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2088, Dec. 1997.
[12] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated *LC* VCOs," *IEEE J. Solid-State Circuits*, vol. 36, pp. 896–909, June 2001.
[13] *Star-Hspice Manual, Release 1998.2*, Avant Corporation, 1998.
[14] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential *LC* oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 717–724, May 1999.
[15] T. Tsukahara, M. Ishikawa, and M. Muraguchi, "A 2 V 2 GHz Si-bipolar direct-conversion quadrature modulator," *IEEE J. Solid-State Circuits*, vol. 31, pp. 263–267, Feb. 1996.

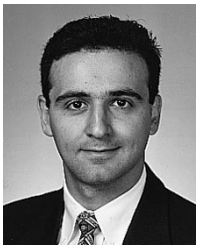
[16] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, "CMOS mixers and polyphase filters for large image rejection," *IEEE J. Solid-State Circuits*, vol. 36, pp. 873–887, June 2001.
[17] S. Navid, F. Behbahani, A. Fotowat, A. Hajimiri, R. Gaethke, and M. Delurio, "Level-locked loop: A technique for broadband quadrature signal generation," in *CICC Dig. Tech. Papers*, 1997, pp. 411–414.
[18] A. Rofougaran, J. Rael, M. Rofougaran, and A. Abidi, "A 900 MHz CMOS *LC*-oscillator with quadrature outputs," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1996, pp. 392–393.
[19] E. Hegazi, H. Sjoland, and A. Abidi, "A filtering technique to lower *LC* oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1921–1930, Dec. 2001.



Roberto Aparicio (S'01) was born in Puebla, Mexico, in 1975. He received the B.S. degree in electronics from Universidad Autonoma de Puebla, Mexico, in 1999 and the M.S. degree in electrical engineering from the California Institute of Technology, Pasadena, in 2001, where he is currently working toward the Ph.D. degree.

His present research interests include *RF* integrated circuits with an emphasis on oscillators, frequency synthesizers and optimization of on chip passive elements. During the summer of 2002, he was with the Mixed-Signal Communications IC Design group at the IBM T. J. Watson Research Center, Yorktown Heights, NY, where he investigated PLL architectures for optical communications.

Mr. Aparicio ranked first at the Universidad Autonoma de Puebla and earned the Phoenix medal in 1998. He was a Fulbright Scholarship and an IBM research fellowship recipient at the California Institute of Technology from 1999 to 2001 and 2002 to 2003, respectively, and received the Walker von Brimer foundation outstanding accomplishment award and the Analog Devices outstanding student designer award, both in 2001.



Ali Hajimiri (S'95–M'98) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from the Stanford University, Stanford, CA.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies (Bell Labs), Holmdel, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, as an Assistant Professor of electrical engineering, where his research interests are high-speed and RF integrated circuits. He is a coauthor of *The Design of Low Noise Oscillators* (Boston, MA: Kluwer, 1999) and has received several U.S. and European patents. He has served as a member of the Technical Program Committees of the International Conference on Computer Aided Design and serves on the Guest Editorial Board of Transactions of the Institute of Electronics, Information and Communication Engineers of Japan.

D. Hajimiri was the Gold medal winner of National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, The Netherlands. He was a corecipient of the International Solid-State Circuits Conference 1998 Jack Kilby Outstanding Paper Award and the winner of the IBM faculty partnership award. He is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II and has served as Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.