10.8 A Bidirectional RF-Combining 60GHz Phased-Array Front-End

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Phased arrays enable electronic steering of the direction of maximum sensitivity of a receiver, providing improved SNR and spatial selectivity [1]. While RF-combined arrays are desirable due to low area and power consumption, they are challenging to implement in silicon due to the need for RF phase shifters. However, multiple-beam-based approaches can be used to simplify array design and enable RF signal combining [2]. This paper presents a 60GHz RF-combined array architecture that adopts a hybrid parallel/series phase-shift approach which reduces the requirements of on-chip phase shifters and provides for simultaneous illumination of two angles of incidence. The 4-element array includes amplitude control in each element as well as continuous phase adjustment.

Figure 10.8.1 shows the block diagram of the RF-combining receiver front-end that incorporates both parallel and series phase-shift techniques. A signal arriving at the n^{th} element in the array with angle of incidence ϕ, will experience a phase shift $\psi_n=(n\text{-}1)\ \pi \sin(\phi)=(n\text{-}1)\psi_o$, assuming antenna spacing of $\lambda/2$. The parallel phase shifters in each element introduce a phase shift $\alpha_n=n\alpha_0$. The signals are then fed into bidirectional series phase shifters, each providing a phase shift of θ. Signals on the series phase shifters travel in both directions, yielding the following signal summations at OutA and OutB:

$$I_{RFA} = I_o \sum_{n=1}^{N} e^{-j[(n-1)\psi_o + n\alpha_0 + (n-1)\theta]} \quad (1)$$

$$I_{RFB} = I_o \sum_{n=1}^{N} e^{-j[(n-1)\psi_o + n\alpha_0 + (N-n)\theta]}, \quad (2)$$

From (1) and (2), it can be shown that the incident angles of maximum sensitivity at OutA and OutB are:

$$\phi_{max,A} = \arcsin\left(\frac{-(\alpha_0+\theta)}{\pi}\right) \text{ and } \phi_{max,B} = \arcsin\left(\frac{-(\alpha_0-\theta)}{\pi}\right) \quad (3)$$

In a classic parallel-fed array, $\theta = 0^\circ$, and hence α_0 needs to vary from -180° to +180° to achieve full spatial coverage. In a series-fed array, where $\alpha_0 = 0^\circ$, OutA and OutB receive signals from two different angles, and hence a 0° to +180° variation in θ ensures full spatial coverage. While the phase-variation requirements of RF phase shifters are reduced in the series-fed array, implementing bidirectional variable phase shifters (BVPs) in silicon that provide 180° of variable phase shift with good linearity, controlled impedance, and uniform gain can be challenging at 60GHz.

In this work, the series-fed and parallel-fed array architectures are combined to further relax the RF-phase-shifter requirements. As shown in Fig. 10.8.1, discrete phase shifters (DPs) in every element choose one of two phase-shift settings, e.g., 0° or 180° in the second element. The DPs can be configured to provide different values of α_0 in each mode of operation, thereby reducing the variable-phase-shift requirement in the BVPs. For example, if the DP settings permit two array modes, with $\alpha_0 = 0^\circ$ and $\alpha_0 = 180^\circ$, it can be shown from (3) that the BVP variable-phase-shift requirement is reduced to 90°. In this work, DPs are implemented such that the array has four modes (Fig. 10.8.2), leading to a BVP variable-phase-shift requirement of only 45°. Figure 10.8.2 shows the angles of maximum sensitivity in the ψ_0-plane and in the ϕ-plane for OutA and OutB, when the BVP phase shift is varied from 135° to 180°. Though the directions received at OutA and OutB are different, they are not independent of each other in this implementation. However, the architecture can be extended to receive from any two given directions by replacing the DPs with variable phase shifters, thereby acquiring another degree of freedom. Furthermore, the hybrid parallel/series-array architectures can be generalized to broadband true-time-delay arrays, as the adjacent coupling and reuse of time-delay elements can reduce delay-variation requirements.

Next, the functioning of the array and the design challenges, particularly in the BVP, are discussed in depth. The input to each element is first amplified by a 60GHz LNA that has variable gain to compensate for downstream gain variations. The LNA is a 4-stage design, in which the first 3 stages are similar to [3] while the 4th stage provides variable gain by current steering. The output of the LNA is provided to a DP that can choose between two phase-shift settings (Fig. 10.8.3). The discrete phase shift in each element is achieved using a combination of transmission lines and a passive 180° phase inverter. The DP output is converted to current by a transconductance stage (G_m-stage) whose output impedance is much higher than the impedance of the BVPs to which it is coupled (Fig. 10.8.3). Hence, when the impedances at OutA and OutB are matched to that of the BVPs, the output of each G_m-stage sees two equal parallel loads to the left and right, causing the output current from each element to divide equally between OutA and OutB. The BVPs are matched to 50Ω at OutA and OutB using a $\lambda/4$ transformer with the G_m-stage functioning as an open-drain stage.

The BVP is implemented using multiple sections of capacitively loaded transmission lines in which the phase shift is varied using MOS varactors (Fig. 10.8.4). In order to provide design insight, the BVP sections are approximated as LC sections to derive the equations in Fig. 10.8.4. It can be seen that for phase-shift variation from 180° to 360°, the varactor capacitance has to vary by at least a factor of 4; moreover the bandwidth decreases with increasing phase shift, leading to higher loss. Additionally, in such a BVP the impedance changes with phase shift, necessitating variable load impedance in order to maintain power matching. Thus, the reduction in the BVP variable-phase-shift requirement to 45° results in lower phase-shifter loss while also ensuring that a constant load impedance at OutA and OutB provides sufficiently good output match across phase-shift settings. The measured phase shift and insertion loss at 60GHz for a 5-section BVP stage are shown in Fig 10.8.4. Measurements on a standalone BVP indicate S_{11} <–20dB for 25Ω terminal impedances across all phase-shift settings.

Figure 10.8.5 shows the measured input and output match, gain and noise figure of the front-end. While the gain variation for different DP settings is within 1.2dB, it is larger across BVP settings (Fig. 10.8.5b). This can be compensated substantially by the 10dB gain variation in the variable-gain LNA. The noise figure of the front-end varies from 5.3dB (Input 4 → OutB) to 6.9dB (Input 1 → OutB) at 60GHz. Since the noise figure of the receiver is dominated by the LNA and the subsequent blocks before the BVP, this phased-array architecture provides an improvement in SNR despite the reuse of series BVPs. The front-end input-referred P_{1dB} is –33.5dBm.

Figure 10.8.6 shows the 4-element array patterns based on measured S-parameters which closely match theoretical predictions in Fig. 10.8.2. The array achieves full spatial coverage with a peak-to-null ratio higher than 25dB. Figure 10.8.7 shows a die micrograph of the array which is implemented in a 0.12µm SiGe BiCMOS process. In each element, the LNA draws 12mA from 2.7V while the other circuits draw 10mA from 2.7V and 3mA from 2.2V. The 4-element front-end consumes 265mW and occupies 1.85×2.5mm² of die area.

Acknowledgments:
The authors wish to thank U. Pfeiffer, B. Gaucher, and S. Weinreb. Partial funding for this work was provided by DARPA (N66001-02-C-8014-A).

References:

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[3] B. Floyd, S. Reynolds, U. Pfeifer, T. Beukema, J. Grzyb, and C. Haymes, "A Silicon 60GHz Receiver and Transmitter Chipset for Broadband Communications," *ISSCC Dig. Tech. Papers*, pp. 184-185, Feb., 2006.

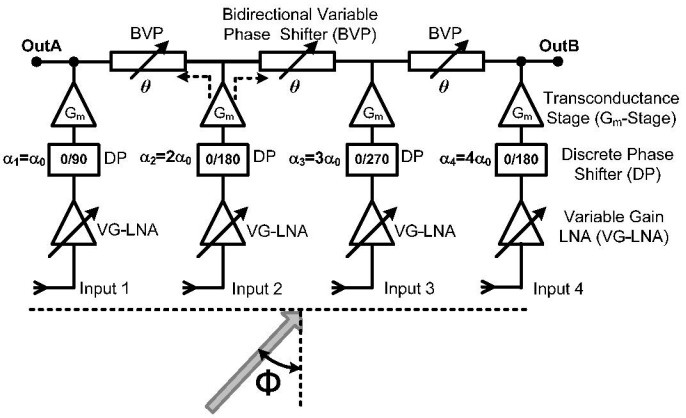

Figure 10.8.1: Bidirectional RF-combining phased-array architecture.

Discrete phase shifter settings leading to different α_0 in each mode

Mode \ Element	1	2	3	4
1	0°	0°	0°	0°
2	90°	180°	270°	0°
3	0°	180°	0°	180°
4	90°	0°	270°	180°

Mode	α_0
1	0°
2	90°
3	180°
4	-90°

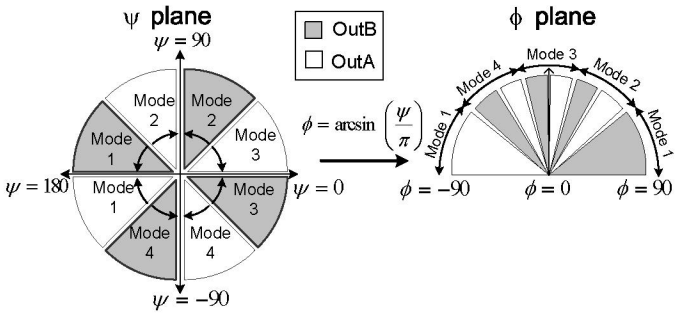

Figure 10.8.2: Angles received in each array mode (BVP variation:135°to 180°).

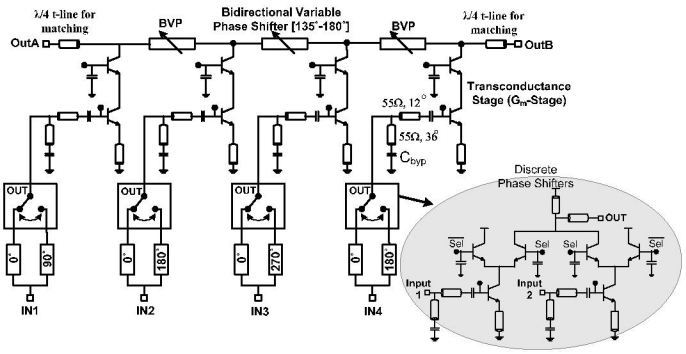

Figure 10.8.3: Discrete phase shifters (DPs) and transconductance stage.

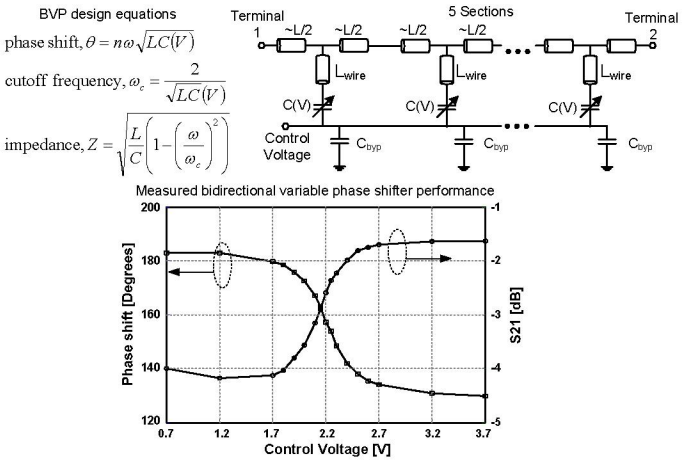

Figure 10.8.4: 60GHz bidirectional variable phase shifter (BVP).

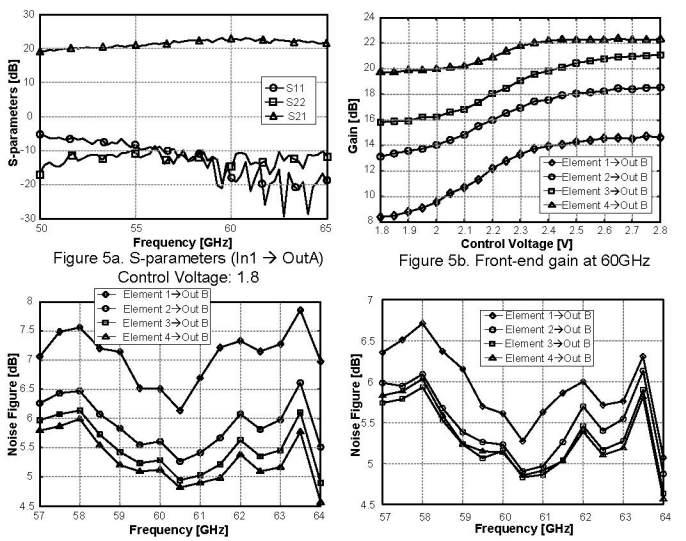

Figure 5a. S-parameters (In1 → OutA) Control Voltage: 1.8

Figure 5b. Front-end gain at 60GHz

Figure 10.8.5: Measured 60GHz front-end performance.

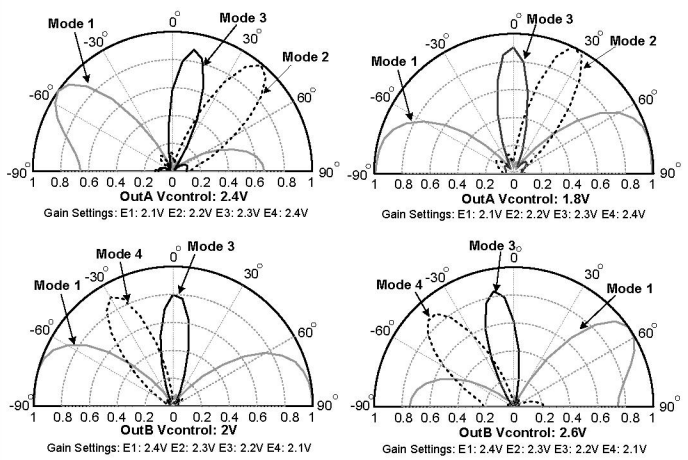

Figure 10.8.6: Normalized 4-path array pattern for OutAand OutB (gain-control and phase-control settings as indicated).

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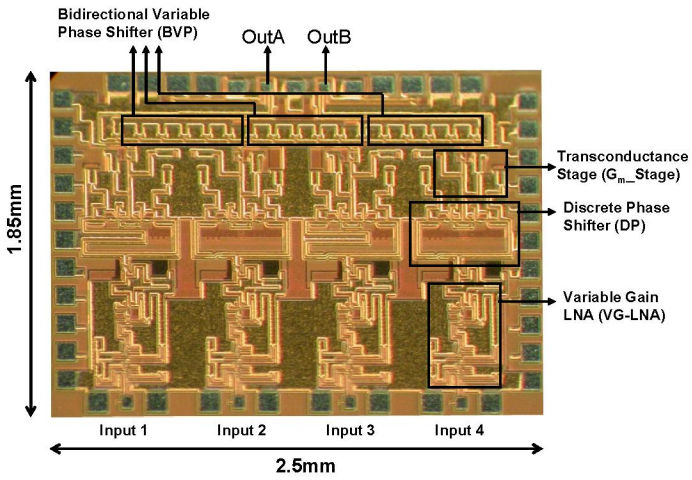

Figure 10.8.7: Die micrograph of 60GHz phased-array front-end.

