

A Breakdown Voltage Multiplier for High Voltage Swing Drivers

Sam Mandegaran, *Student Member, IEEE*, and Ali Hajimiri, *Member, IEEE*

Abstract—A novel breakdown voltage (BV) multiplier is introduced that makes it possible to generate high output voltage swings using transistors with low breakdown voltages. The timing analysis of the stage is used to optimize its dynamic response. A 10 Gb/s optical modulator driver with a differential output voltage swing of 8 V on a 50 Ω load was implemented in a SiGe BiCMOS process. It uses the BV-Doubler topology to achieve output swings twice the collector-emitter breakdown voltage without stressing any single transistor.

Index Terms—Breakdown voltage (BV), breakdown voltage doubler, BV-Doubler, breakdown voltage multiplier, BV-multiplier, driver, optical modulator driver, SiGe.

I. INTRODUCTION

RECENTLY, there has been a great deal of interest in silicon-based high-speed integrated circuits for wire-line communications due to cost advantages and integration prospects. While most of the building blocks in a fiber optics transceiver have been implemented and demonstrated in silicon at 10 Gb/s and above [1]–[6], the optical modulator electrical driver, for output voltages over 3 V_{pp}, has been primarily done in compound semiconductors [7]–[11]. This is mainly due to breakdown limitations of silicon transistors and large required voltage swings of today's high-speed optical modulators. Furthermore, the process technology disparity between the driver and the rest of the transceiver results in additional cost and performance penalties. This paper introduces a breakdown voltage (BV) doubler topology that overcomes the breakdown limitations of the transistors by design and enables high-speed broadband drivers with a large voltage swing in silicon.

Existing electro-absorption and Mach-Zehnder (MZ) optical modulators require voltage swings typically in the range of 4–8 V to achieve a high extinction ratio, i.e., to switch the light on and off effectively. Such a large voltage swing poses a challenge for silicon-based transistors (SiGe HBT [6], [7], [12]–[14] or Si CMOS [15]) whose breakdown voltages are constantly dropping with continuous scaling for higher speed. While there have been reports of driver circuits in SiGe for optical applications, most of these circuits drop the entire voltage swing across single transistors and thus cannot exceed the collector-emitter breakdown voltages, and are, hence, limited to a voltage swing of around 3 V. Kanda *et al.* used a driven-cascode topology in InP HEMT without the timing adjustment

capacitor [16], and Li and Tsai [17] have recently demonstrated additional improvement to our original proposed BV-Doubler topology [20]. A self-biased cascode has been used for RF power amplifiers to alleviate the breakdown voltage problem [18]. Li and Tsai have recently demonstrated a self-biasing modulator driver in CMOS [19], and low-frequency examples of stacked CMOS with varying gate voltages have been demonstrated in [20], [21]. Table I compares these works. This paper offers a 10 Gb/s modulator driver with a novel BV-Doubler (Multiplier) topology that can generate output voltage swings twice (multiple times) the transistor breakdown voltages, without exceeding the nominal operation conditions of any of the active devices in the circuit [22]. Fig. 1 shows the main idea and topology. The BV-Doubler topology can be viewed as a switch that can tolerate output voltage swings up to twice the transistor breakdown voltage, BV_{CER} . Section II investigates the breakdown mechanisms in bipolar transistors. Section III describes the evolution of the main idea. In Section IV, the DC design considerations are described. Section V generalizes the idea to a BV-Multiplier, and Section VI provides a complete timing analysis of the design. Sections VII and VIII present the experimental results.

II. BREAKDOWN VOLTAGE

One of the main limiting factors for using silicon for high-speed drivers is the low breakdown voltage of fast silicon-based transistors. As transistors become faster, due to scaling, they subsequently become less tolerant of high voltages. In a bipolar implementation, the breakdown voltage that is of most concern for a driver circuit is the breakdown voltage across emitter and collector, BV_{CE} . For driver design, the distinction between the two different BV_{CE} values reported is important. One is BV_{CEO} , and the other BV_{CER} . BV_{CEO} corresponds to the breakdown voltage of the collector-emitter when the base is open. BV_{CEO} is the most commonly reported value since it corresponds to the worst case scenario (it is the lowest); however, it is of little value for driver design. The important values are BV_{CER} , which is the breakdown voltage of the collector-emitter junction with a specified finite base resistance.

The physical explanation of the dependence of BV_{CE} on the base impedance is as follows. Let us first consider the open base case for an NPN transistor with a voltage applied to the collector and emitter such that the collector is at higher potential. Ideally, if the voltage across the collector and emitter is small enough, the current through the collector and emitter should be equal to the reverse saturation current of the base-collector junction. This reverse saturation current injects holes generated in the collector-base depletion region into the base, where they

Manuscript received January 19, 2005; revised August 8, 2006.

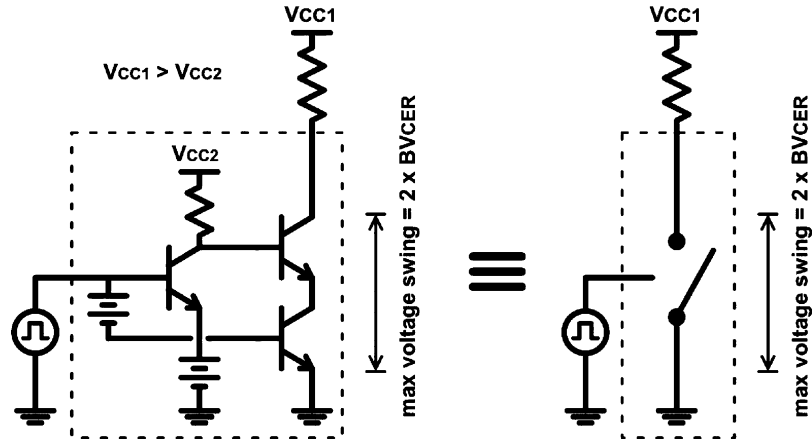
S. Mandegaran was with the California Institute of Technology, Pasadena, CA 91125 USA. He is now with Raytheon, Pasadena, CA 91101 USA, and also with the University of Southern California School of Cinematic Arts, Los Angeles, CA 90089 USA.

A. Hajimiri is with the California Institute of Technology, Pasadena, CA 91125 USA (e-mail: hajimiri@caltech.edu).

Digital Object Identifier 10.1109/JSSC.2006.889390

TABLE I
 COMPARISON OF MODULATOR DRIVERS

| Ref. | Technology | Speed (Gb/s) | Output Swing – Single Ended (V _{pp}) |
|-----------|-------------|--------------|--|
| [6] | SiGe BiCMOS | 20 | 3.2 |
| [7] | SiGe | 14 | 3.6 |
| [8] | InGaP/GaAs | 10 | 5.5 |
| [9] | InP | 12.5 | 3.1 |
| [10] | GaAs | 10 | 14 |
| [11] | GaAs | 10 | 7.4 |
| [12] | SiGe | 40 | 2.5 |
| [13] | SiGe | 23 | 3.5 |
| [14] | SiGe BiCMOS | 14 | 3.3 |
| [15] | CMOS | 10 | 2 |
| [17] | SiGe BiCMOS | 10 | 4.5 |
| [19] | CMOS | 10 | 4 |
| This work | SiGe BiCMOS | 10 | 4 |


 Fig. 1. BV-Doubler topology, which is equivalent to a switch that can tolerate an output voltage swing up to $2 \times BV_{CER}$.

are majority carriers and move to the edge of the base–emitter depletion region, narrowing the base–emitter depletion region. The narrower depletion region corresponds to a smaller barrier, which will allow more electrons to be injected into the base region. These electrons will be absorbed by the base–collector depletion region, where they accelerate due to the electric field. As the voltage across the collector and emitter is increased, there will be a wider base–collector depletion region, thus accelerating electrons to high enough velocities to ionize other atoms and producing new electron–hole pairs. The new holes will further narrow the base–emitter depletion region and make the barrier even smaller, causing more electrons to be injected into the base region. This will lead to an avalanche breakdown [23], [24]. Now if the base is connected to low impedance, some of the holes generated in the base–collector junction can be taken out of the base before reaching the base–emitter depletion region. This can delay the avalanche breakdown, and we get the following relationship:¹

$$BV_{CEO} < BV_{CER} < BV_{CER} \Big|_{R=0}$$

¹In the case of the process used for this project, BV_{CEO} was 1.8 V and BV_{CER} was >3.0 V for $R_{Base} < 100 \Omega$.

In most high-speed drivers, the entire output voltage swing is across the emitter–collector of one transistor. For these circuits, even for very low R_B , BV_{CER} is still not high enough to accommodate many high-speed driver applications such as 10/40 Gb/s optical MZ modulators. Most such modulators require voltage swings well in excess of 3.0 V.

III. CIRCUIT CONCEPT

In this section, we offer a solution to achieve high output voltage swings despite the low BV of high-speed transistors. This solution will allow output voltage swings up to twice BV_{CER} , which we will name BV-Doubler. We will then generalize this concept to achieve even higher voltage swings in Section V.

The first thing that comes to mind is to divide the output voltage swing between two transistors. This will immediately resemble a standard cascode topology, as shown in Fig. 2(a). However, a standard cascode topology does not divide the output voltage equally on both transistors at all times. In a standard cascode topology the base of the upper transistor, Q_{C2} , is kept at a constant voltage, V_{BIAS} . Due to the exponential dependence of the collector current on the base–emitter voltage of the bipolar transistor, the voltage of the emitter of Q_{C2} , node

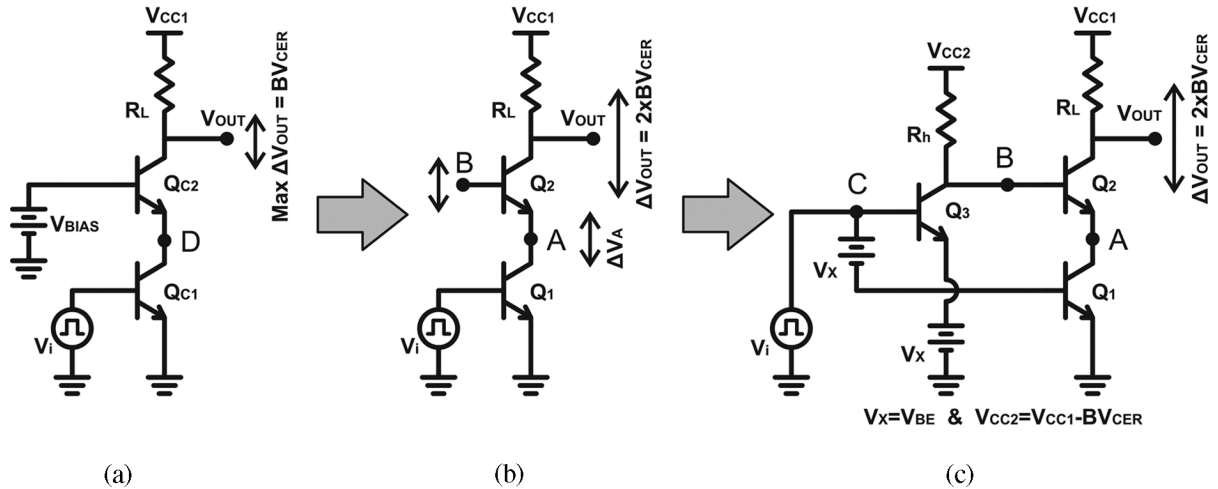


Fig. 2. The evolution from (a) a standard cascode, to (b) a base driven cascode, to (c) the BV-Doubler topology.

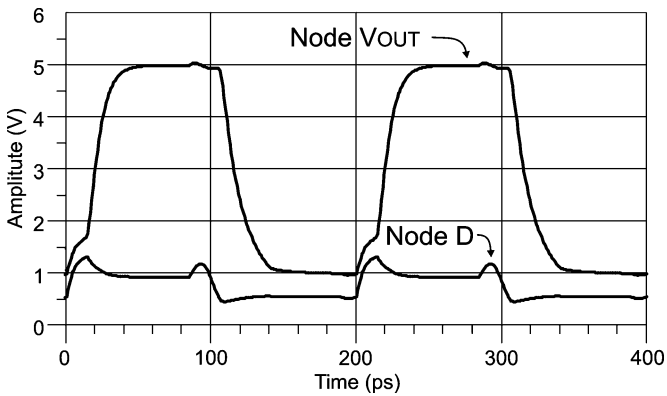


Fig. 3. Simulation of the cascode circuit in Fig. 1(a). This simulation shows that in a standard cascode, almost the entire output voltage swing appears across the top transistor.

D, remains relatively constant. Thus, almost the entire voltage swing appears across only the upper transistor, Q_{C2} . Fig. 3 shows a simulation of the cascode in Fig. 2(a). It can be seen in Fig. 3 that most of the output voltage swing is dropped across the top transistor Q_{C2} .

To solve this problem, we should vary the voltage of the base of the upper transistor. If this is done in synchronous with the output voltage, it will be possible to divide the output voltage equally on the collector–emitter of two transistors, Q_1 and Q_2 , as shown in Fig. 2(b). The length of the arrows in Fig. 2, qualitatively represent the magnitude of the voltage swing. If the output voltage swing is V_{OUT} , then in order to divide the voltage equally on the two transistors Q_1 and Q_2 , node A must have a voltage swing half of the output voltage swing, i.e.,

$$\Delta V_A = \Delta V_{OUT}/2.$$

Taking into account the difference between the on and off base–emitter voltages ($V_{BE,ON}$ versus $V_{BE,OFF}$) of Q_2 , the voltage at the base of Q_2 will have to vary by

$$\Delta V_{B,Q2} = \Delta V_A - (\Delta V_{BE,ON} - \Delta V_{BE,OFF}).$$

One way to accomplish this voltage swing on the base of Q_2 is to use a common-emitter configuration to drive the base of Q_2 , as shown in Fig. 2(c). Transistor Q_3 will be turned on and off completely just as Q_1 and Q_2 , and all transistors will be turned on and off synchronously. When transistor Q_3 is off, voltage V_{CC2} determines the upper voltage of node B, and when Q_3 is on, the voltage drop across R_h , i.e.,

$$V_{Rh} = I_{E,Q3} \cdot R_h$$

determines the lower voltage of the base of Q_{C2} . At this point, we have been able to divide the output voltage swing between the two transistors, Q_1 and Q_2 , in all modes of operation. This is the basic low-frequency BV-Doubler topology. The overall BV-Doubler can be viewed as a switch that can tolerate an output voltage swing $2 \times BV$. This is shown in Fig. 1.

If the BV-Doubler circuit is implemented as shown in Fig. 2(c), the delay mismatch between the two signal paths will result in degraded output waveform. The output wave will have noticeable kinks in it, as shown in Fig. 4(b). This output waveform will result in degraded eye diagram and thus high bit-error rate (BER). This poor waveform is caused by timing mismatch. As shown in Fig. 4, the signal takes two paths to the output. The path through Q_3 is the faster path, mainly due to the fact that the output resistance of Q_1 which is around 350Ω in our implementation, acts as emitter degeneration for Q_2 trading gain for bandwidth, resulting in a faster response. The signal arrives at the output at different times, which causes kinks on the output waveform. In order to correct the output waveform, the upper path must be slowed at the base of Q_2 . This can be accomplished by introducing a capacitor, C_h , at node B. By choosing an appropriate value for C_h , the two paths will have equal time lags and thus the two signals will arrive at the output node synchronously, improving the quality of the output waveform.

Fig. 5 shows the simulation results that illustrate the behavior of the slow and the fast paths. Transistors Q_1 and Q_3 are driven by ideal voltage pulses. Fig. 5(b) shows the output voltage when the two voltage sources, V_{i1} and V_{i2} , are synchronous. There are noticeable kinks in Fig. 5(b) due to different response time of

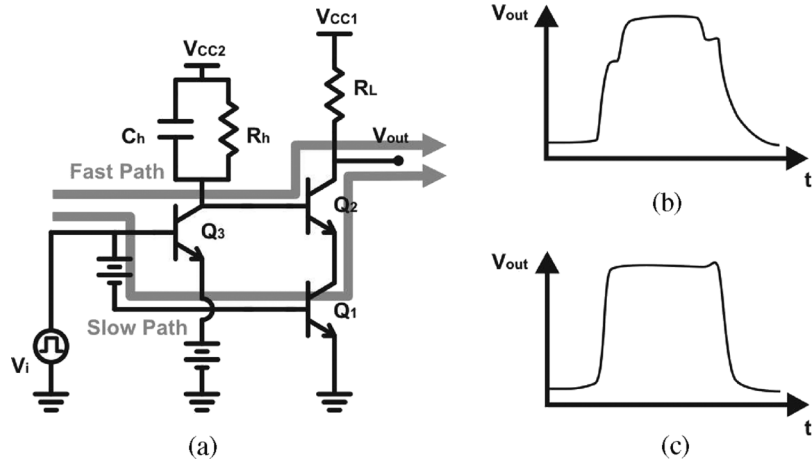


Fig. 4. (a) There are two signal paths to the output node. (b) Output waveform without capacitor C_h , and (c) with capacitor C_h .

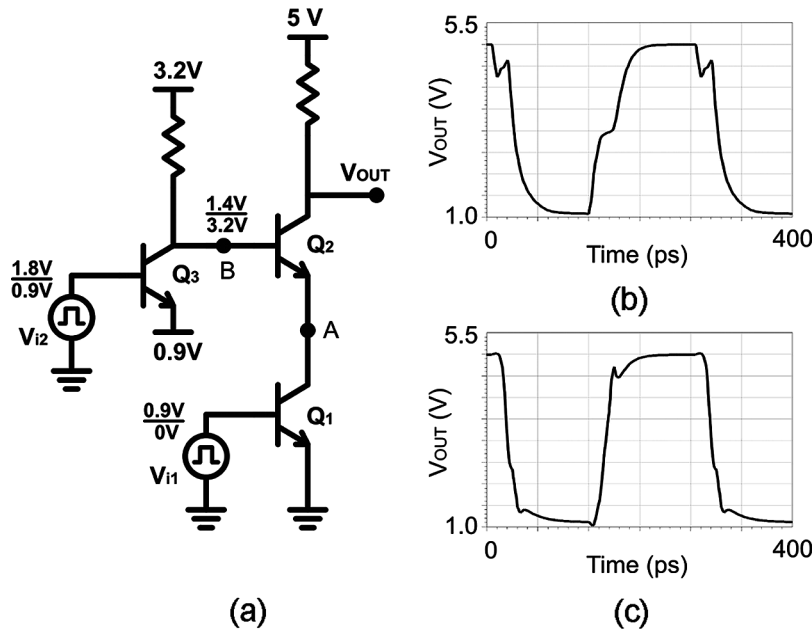


Fig. 5. Simulation results with ideal voltage sources. (a) shows the bases of Q_1 and Q_3 driven by voltage sources V_{i1} and V_{i2} , and the voltage levels are shown in the graphs. (b) shows V_{OUT} with V_{i1} and V_{i2} in sync. (c) shows V_{OUT} with V_{i2} delayed 20 ps compared to V_{i1} . Both voltage sources are square waves with 100-ps pulse width.

transistors Q_1 and Q_2 . Fig. 5(c) shows the output voltage when the upper voltage source, V_{i2} , is delayed by 20 ps compared to the lower voltage source, V_{i1} . This results in faster and more monotonic rising and falling edges. In Fig. 4, capacitor C_h acts as a delay element to slow the signal at the base of Q_2 . The addition of an appropriate size C_h is equivalent to delaying the base of Q_2 by 20 ps to achieve the best rise and fall time at the output node.

Without the capacitor C_h , the output voltage does not equally divide between the collector and emitter of the two output transistors Q_1 and Q_2 at all times. Fig. 6 shows the voltages at nodes A and B in comparison with V_{OUT} with C_h on node B, which synchronizes the voltages of the three nodes, equally dividing the output voltage swing between the Q_1 and Q_2 . The necessary large spikes of charge at the base of Q_2 necessary during the transitions to charge and discharge the base of Q_2 is provided by the C_h that acts as a reservoir. A more detailed analysis of

the circuit and the effect of C_h is presented in Section V, which shows the feasibility and robustness of this approach.

IV. CIRCUIT DESIGN

In this section, the specifics of the prototype BV-Doubler demonstrated in this paper are reviewed. For this design, we chose a very conservative maximum BV_{CER} of 2.5 V. To avoid saturation, we made sure that the voltage of the collector-emitter never went below 0.5 V. This left about 2 V of voltage swing per transistor. Using two transistors, a single-ended voltage swing of 4 V could be accomplished. Fig. 7 shows the voltages of all nodes for both when the transistors are on and when they are off. The SiGe BJTs used for this design have a $V_{BE,ON}$ of approximately 0.9 V for typical current levels; however, even though all transistors are of the same type, during the operation of this circuit, the $V_{BE,OFF}$ of Q_2 is different than Q_1 and Q_3 . In Q_1 and Q_3 , $V_{BE,OFF}$ is

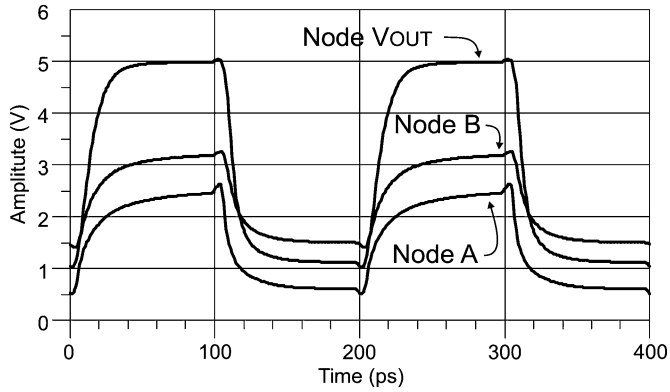


Fig. 6. Voltages of nodes V_{OUT} , A, and B with capacitor C_h in the circuit. This graph shows that node B is half the value of V_{OUT} through the entire switching period and thus the output voltage is equally divided between the two output transistors Q_1 and Q_2 .

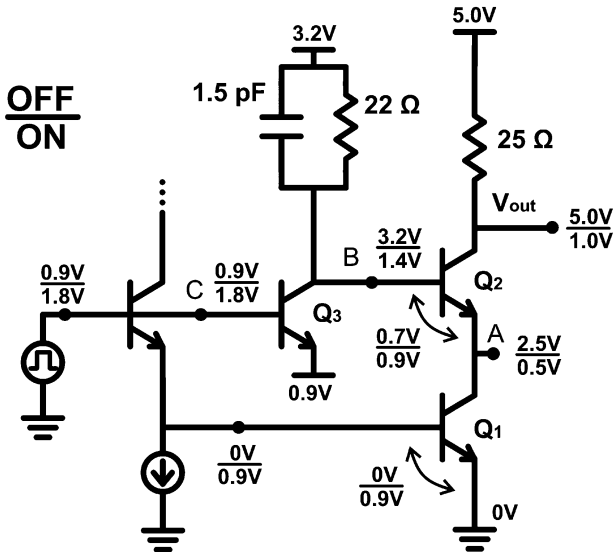


Fig. 7. Voltages of every node in the on and off state.

forced to be zero; however, for Q_2 since the emitter is floating (it is connected to the collector of Q_1 , a high impedance node), $V_{BE,OFF}$ is about 0.7 V. This difference in $V_{BE,OFF}$ of the transistors is important in designing the base driving portion, which will include setting the values for R_h and V_{CC2} .

The input impedance of a MZ modulator is often designed to be a 50Ω resistor to ground. Two on-chip 50Ω resistors were used to match the load and prevent reflection from the 50Ω transmission lines connecting the chip to the modulator. Therefore, the overall resistance seen at the collector of Q_2 is 25Ω . In order to achieve a voltage swing of 4 V at the output node, a total current of 160 mA is required. Fig. 7 shows the voltages V_{OUT} and node A in on and off states. The extra 0.5 V on node A is to avoid saturation. The emitter of Q_1 is kept at a constant 0 V. The voltages of node A and considering $V_{BE,ON}$ and $V_{BE,OFF}$ of Q_2 will determine the desired two voltages for node B to be 3.2 V and 1.4 V. The two voltage levels of node B are set by V_{CC2} , R_h , and $I_{C,Q3}$. When the transistor Q_3 is off, $I_{C,Q3}$ will be zero; consequently, the voltage drop across R_h will be zero and the voltage of node B will be equal to V_{CC2} . When Q_3 is

on, the voltage of node B will be V_{CC2} minus the voltage drop across R_h . In choosing R_h and $I_{C,Q3}$, care must be taken so that R_h is small enough to achieve the desired BV_{CER} . R_h was set to 22Ω (which was a somewhat arbitrary value yet small enough to satisfy the resistance required for the desired BV_{CER}). Consequently, the current through Q_3 was set to 80 mA to achieve the 1.8 V across R_h . The voltage that turns Q_3 on and off at node C is lowered with an emitter-follower and fed to the base of Q_1 ; in this manner Q_1 and Q_3 simultaneously switch on and off.

After the chip was fabricated, it became evident that R_h was chosen unnecessarily small, which made the current through Q_3 unnecessarily large. A larger R_h of about 90Ω would have worked as well. In this case, the current in Q_3 would have been reduced from 80 mA to 20 mA, which would have significantly reduced the power consumption.

The actual circuit is implemented as a fully differential stage, as depicted in Fig. 8. Several emitter-followers precede the main driver stage to lower the source impedances and provide the appropriate DC levels to both main and auxiliary paths. The pre-driver stage is a differential pair. It generates the 0.9 V swing needed at the input of the main driver stage, while the input of the circuit can be anywhere between 0.2–1.0 V. Additional resistors and diodes are used in the collectors of these emitter-followers to avoid excessive V_{CE} and potential breakdown problems. The output driver consists of a main differential cascode path and an auxiliary differential path with timing adjustment capacitors C_h on each side. The resistor R_D lowers the common-mode DC level seen by the auxiliary path, while it has no effect on the differential signal as node D is virtual ground. Capacitor C_D is used to lower the common-mode impedance on node D to suppress even-mode variations. In the next section, a detailed analysis of the BV-Doubler stage will be offered.

V. ANALYSIS

In this section, we perform a small-signal analysis of the output stage dynamics. Even though this circuit operates with large signals going beyond the linear region of the transistors, a small-signal analysis can be used to gain insight into the dynamics of the circuit, which will help understand and improve the performance of the circuit. Small-signal analysis can provide accurate estimates of the switching stages, as the most sensitive part of the switching operation for an ECL-type circuit occurs during the linear steering of the stage. It was shown in [25] and [26] that a pencil-and-paper calculation of a linearized small-signal analysis of an ECL (which operates in the large-signal regime) can give results with errors smaller than 20%. A more detailed justification for use of small-signal analysis to approximate the switching time of ECL-type devices is given in [27].

Fig. 9 is a simplified half-circuit small-signal equivalent of the output stage. The forward signal path consists of two parallel paths with different dynamics, the main path and the auxiliary path. The transfer functions of these paths will be derived.

A. Main Path

The main path consists of an emitter-follower buffer whose dynamics is nondominant, followed by the common-emitter

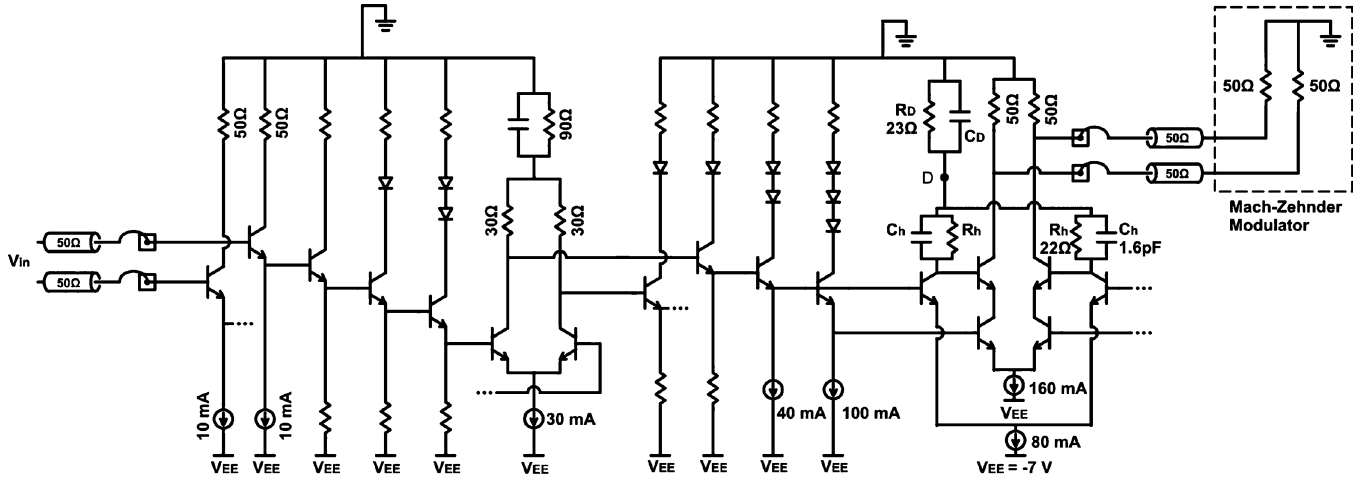


Fig. 8. Full schematic of the implemented circuit. A differential form of the BV-topology was used.

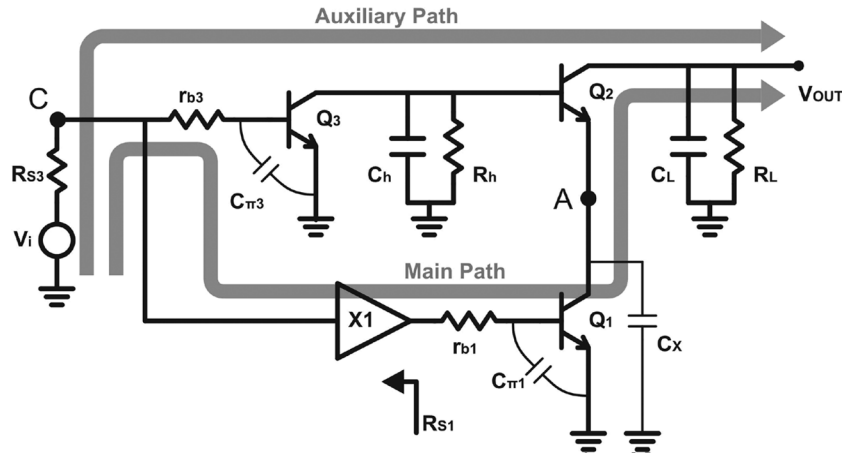


Fig. 9. Half-circuit small-signal equivalent of the output stage.

transistor, Q_1 , and the common-base transistor, Q_2 , driving the output node. It has an inverting small-signal DC gain of

$$A_1 = -g_{m1}R_L \quad (1)$$

where g_{m1} is the transconductance of Q_1 and R_L is the output load resistance. In our design, for an average $g_{m1} \approx 3.2 \Omega^{-1}$ and $R_L = 25 \Omega$, we obtain $A_1 \approx -80$.

The dynamics of the main path is dominated by the pole at the input of Q_1 , $p_{\pi 1}$, approximately given by

$$p_{\pi 1} \cong \frac{-1}{C_{\pi 1}[(R_{S1} + r_{b1})||r_{\pi 1}]} \approx \frac{-1}{C_{\pi 1}(R_{S1} + r_{b1})} \quad (2)$$

where R_{s1} is the output resistance of the buffer driving the base, r_{b1} is the physical base resistance of Q_1 , and $C_{\pi 1}$ is the base-emitter capacitance of Q_1 . Since $r_{\pi 1}$ is much greater than $R_{s1} + r_{b1}$, it has a small effect on the pole frequency and it can be ignored. With a total base resistance of $R_{s1} + r_{B1} \approx 7 \Omega$ and $C_{\pi 1} \approx 3.0$ pF, the pole is at ~ 7.6 GHz.

B. Auxiliary Path

The noninverting small-signal DC gain of the auxiliary path is given by

$$A_2 = g_{m3}R_h \cdot \frac{g_{m2}R_L}{1 + g_{m2}r_{o1}} \cong \frac{g_{m3}R_hR_L}{r_{o1}} \quad (3)$$

where g_{m3} and g_{m2} are the transconductances of Q_3 and Q_2 , respectively, and r_{o1} is the output resistance of Q_1 . This path consists of a common-emitter stage with a gain of $-g_{m3} \cdot R_h$ and another highly degenerate common-emitter with a gain of $-R_L/r_{o1}$. The DC gain from the input to the collector of Q_3 , $-g_{m3} \cdot R_h$, is approximately one-half of A_1 to guarantee equal division of the voltage swing at the output, as discussed in the previous section. Our design values are approximately $g_{m2} \approx 1.6 \Omega^{-1}$, $g_{m3} \approx 3.2 \Omega^{-1}$, $r_{o1} \approx 350 \Omega$, resulting in $A_2 \approx 2.5$.

The auxiliary path has slightly more complex dynamics. There are two dominant poles and a zero in the auxiliary path. The first pole is at the input of Q_3 , $p_{\pi 3}$, which is given by

$$p_{\pi 3} \cong \frac{-1}{C_{\pi 3}[(R_{S3} + r_{b3})||r_{\pi 3}]} \approx \frac{-1}{C_{\pi 3}(R_{S3} + r_{b3})} \quad (4)$$

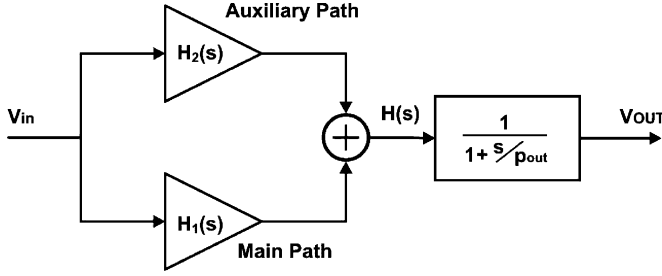


Fig. 10. Equivalent system for the driver.

where R_{S3} is the source resistance of the emitter-follower driving Q_3 and r_{b3} is its physical base resistance.² With a total base resistance of $R_{S3} + r_{B3} \approx 11 \Omega$ and $C_{\pi3} \approx 1.5 \text{ pF}$, the pole is at $\sim 9.6 \text{ GHz}$.

The timing capacitance, C_h , introduces the second pole in the auxiliary path, p_h , which is

$$p_h \cong \frac{-1}{R_h C_h}. \quad (5)$$

Additionally, the total parasitic capacitance on node A, C_x , generates a nondominant pole around the transistor's cut-off frequency, ω_T , and a left-half-plane (LHP) zero at

$$z_x \cong \frac{-1}{r_{o1} C_x}. \quad (6)$$

From simulations, the total parasitic capacitance on node C was determined to be $C_X \approx 2.5 \text{ pF}$, combined with $r_{O1} \approx 350 \Omega$, the zero z_X is located at 180 MHz .

Hence, the transfer function for the main path can be described as

$$H_1(s) = \frac{A_1}{1 + s/p_{\pi1}}. \quad (7)$$

Similarly, the auxiliary path's transfer function is modeled as

$$H_2(s) = A_2 \frac{(1 + s/z_x)}{(1 + s/p_{\pi3})(1 + s/p_h)}. \quad (8)$$

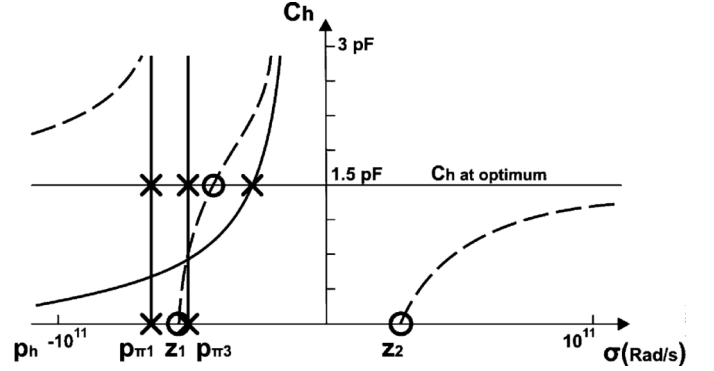
C. Complete System and Effect of C_h

The complete system can be modeled as the parallel combination of these two paths followed by the nondominant output pole, as shown in Fig. 10. Ignoring the nondominant output pole, the equivalent transfer function of the resultant system is

$$\begin{aligned} H(s) &= H_1(s) + H_2(s) \\ &= A \frac{(1 + s/z_1)(1 + s/z_2)}{(1 + s/p_{\pi1})(1 + s/p_{\pi3})(1 + s/p_h)} \end{aligned} \quad (9)$$

where $A = A_1 + A_2$, and z_1 and z_2 are new real zeros. It is noteworthy that the transfer function of the compound system, $H(s)$, has the same poles as $H_1(s)$ and $H_2(s)$, but a different pair of zeros, whose values depend on C_h .

Fig. 11 shows how the real poles and zeros of the overall system move as a function of C_h (y-axis). As can be seen, initially we have a right-half-plane (RHP) zero, z_2 , whose phase contribution can degrade the waveform. Increasing C_h quickly

Fig. 11. Location of poles and zeros as a function of C_h .

pushes this zero to higher frequencies and it eventually becomes a nondominant LHP zero. On the other hand, p_h is initially nondominant but quickly moves in to become dominant. Fortunately, z_1 moves close to p_h , creating a doublet, and hence partially compensating p_h and $p_{\pi3}$ at the optimum point. For the optimal value of $C_h = 1.6 \text{ pF}$, the pole caused by C_h is at 4.5 GHz , and the new zeros are located at $z_1 \approx 6.7 \text{ GHz}$ and $z_2 \approx 0.4 \text{ THz}$. The proximity of z_1 to p_h (doublet) helps to counteract the effect of p_h and overall increase the bandwidth of the system, which consequently improves the output waveform.

VI. GENERALIZED BV-MULTIPLIER

The concept introduced in the last section for achieving output voltage swings twice the breakdown voltage can be generalized to a multiplier. For example, Fig. 12 shows the case for an output swing of $3 \times BV$. In this case, the output voltage swing is divided among three transistors such that each transistor experiences a third of the total voltage swing across its collector-emitter junction, thus achieving an overall voltage swing of $3 \times BV$. The bases of the two top transistors need to be driven. In this case, the base of the middle transistor will swing by approximately $1 \times BV$ and the base of the top transistor by $2 \times BV$. To achieve a voltage swing of $2 \times BV$ for the base of the top transistor, the BV-Doubler topology is used to drive its base. Just as in the BV-Doubler case, the BV-Tripler will need timing adjustment at the bases of the three output transistors to improve the output waveform. This can be corrected by adding capacitors to the load resistors that drive the bases. In principle, this idea can be extended to achieve higher voltage output swings. In general, the timing and voltage level adjustments are more complex in the case of a tripler and merit further studies. Also, eventually the breakdown voltage of the pn-junction between the collector of the top-most transistor and the substrate will be another limiting factor for this generalization.

VII. CIRCUIT IMPLEMENTATION AND LAYOUT

This circuit was fabricated using IBM's $0.18\text{-}\mu\text{m}$ SiGe BiCMOS process 7HP. The NPN transistors had an f_t of 120 GHz . A picture of the fabricated chip is shown in Fig. 13. The dimensions of the chip were 1 mm by 1.2 mm . Only NPN transistors were used in this design. Fig. 14 shows the layout of the chip. The signal flows from left to right and

² $C_{\pi3}$ primarily affects the auxiliary path since r_{b3} is greater than R_{S3} .

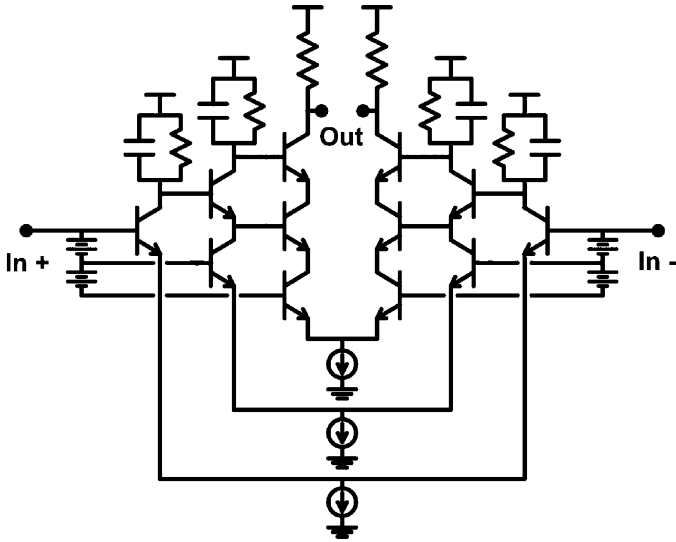


Fig. 12. BV-Tripler. This circuit can achieve single-ended output voltage swing three times the BV, and differentially six times BV.

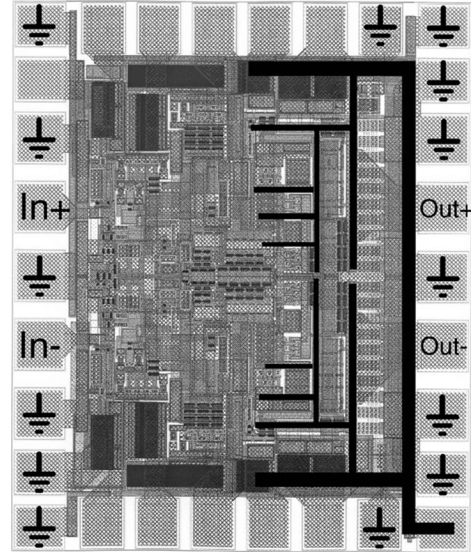


Fig. 14. Layout of the chip. The black solid lines show part of the substrate connections.

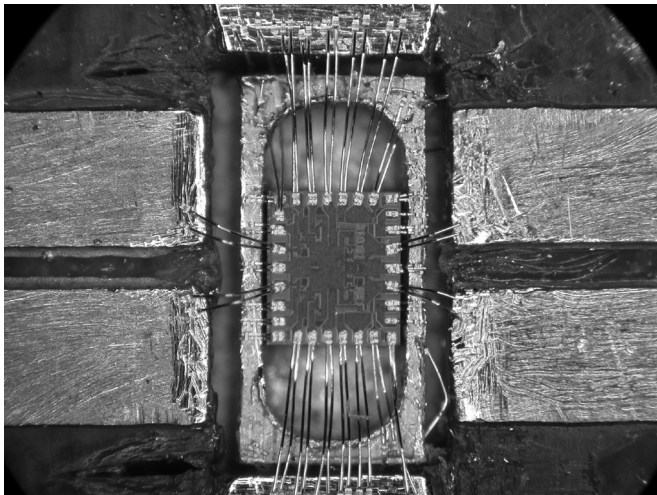


Fig. 13. Chip mounted on a piece of brass. The two left and the two right strips are the differential input and output 50 Ω transmission lines.

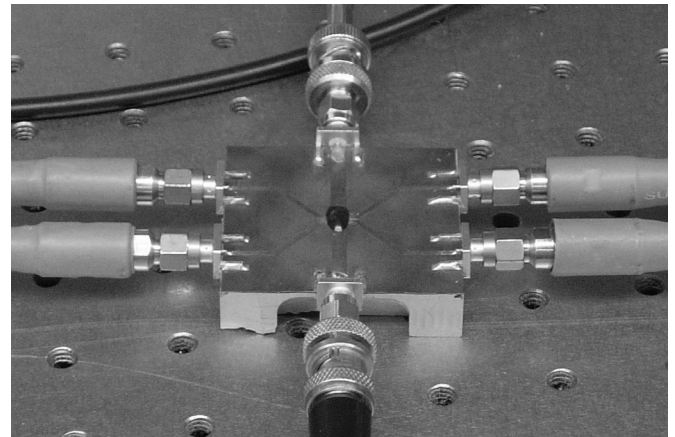


Fig. 15. Chip mounted on a piece of brass. The two left and the two right strips are the differential input and output 50 Ω transmission lines.

both paths go through the center and as close as possible to avoid noise. A dog-bone structure on the top metal layer was used to connect all grounds. Due to very high currents at the output stage, multiple metal layers filled with vias were used to ensure reliable operation. The output matching 50 Ω resistors, seen on the entire right side of the layout in Fig. 14, were p+ polysilicon. These resistors provided the lowest capacitance for a given current. The capacitance on this stage was most crucial to ensure proper operation at 10 Gb/s. The overall capacitances introduced by the 50 matching resistors were about 890 fF.

VIII. EXPERIMENTAL RESULTS

A. Setup

The chip could not be directly mounted on a ground plane because the silicon substrate had to be at a negative supply

relative to ground. Thus, it was placed on a low-cost CVD thick-film diamond (grown by SP3 Diamond Cutting Tools) for good heat dissipation and electrical insulation. The chip and the crystal were then placed on a piece of brass. All three were connected using conductive silver epoxy (Epoxy Tech. H20E). A PCB (Rogers Corp. RT5880) was attached to the brass to carry the signals to and from the chip. As shown in Fig. 13, all the pads were wire-bonded including the signal input and output pads. Input and output wire-bonds were directly connected to 50 Ω transmission lines leading to SMA connectors. Before testing, the chip and the wire-bonds were covered with thermally conductive and electrically insulative epoxy (Epoxy Tech. H70E) to allow for better heat dissipation and protect the die. The chip mounted on a piece of brass covered with epoxy is shown in Fig. 15. The input was differentially fed using a pulse pattern generator (Anritsu MP1763C). The output was connected in many different configurations for both electrical and optical testing. For electrical testing, a

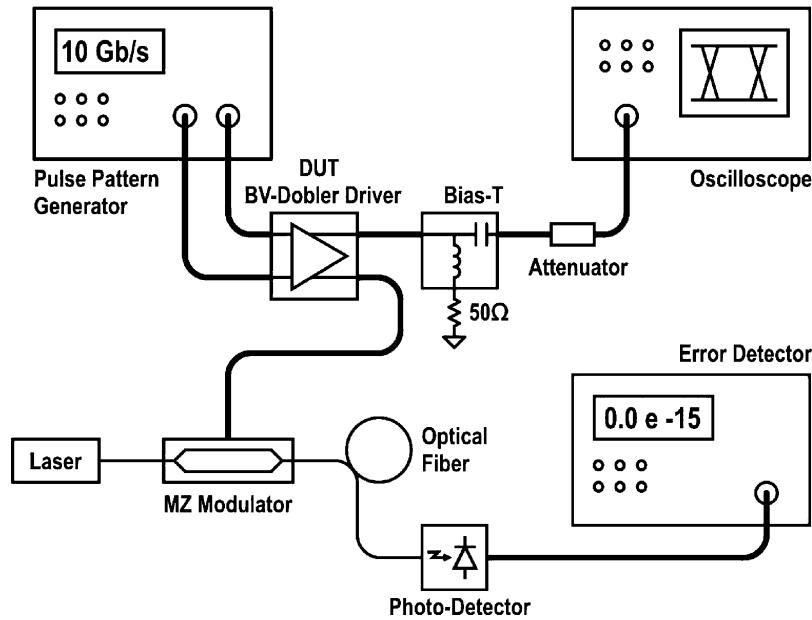


Fig. 16. Test setup. Both electrical and optical test were performed simultaneously.

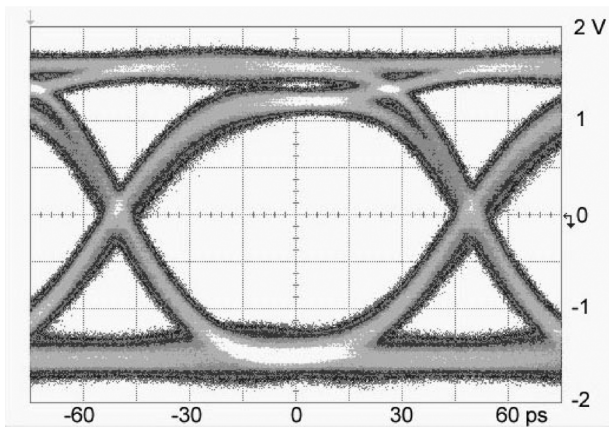


Fig. 17. Electrical eye diagram of one output.

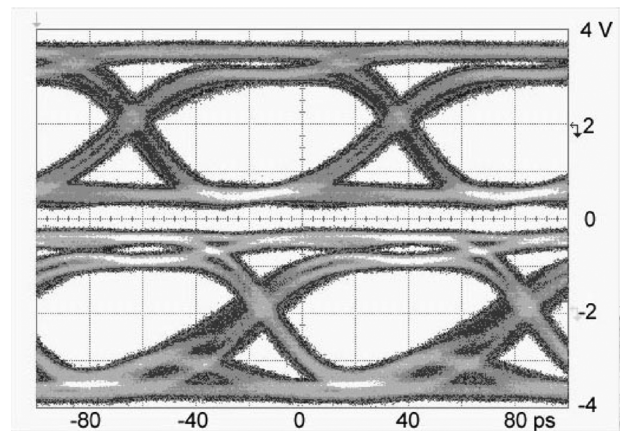


Fig. 18. Electrical eye diagram of the two differential outputs. The bottom output is noisier due to poor substrate connection.

50 GHz oscilloscope sampling head (Agilent 83484A) was used. A diagram of the setup is shown in Fig. 16.

B. Measurements

The measured differential output swing at 10 Gb/s was between 7 and 8 V depending on the power supply voltage. The eye diagram in Fig. 17 is an electrical eye diagram of the single-ended output of the driver with a 3.8 V swing. For Fig. 17, the output signal was connected through a bias-T and a 20 dB attenuator to the oscilloscope. The power supply was -6.5 V and the current drawn was 562 mA. The input signal was differential 10 Gb/s with 250 mV swing on each input. The chip was tested for extended periods both optically and electrically, measuring the BER. No error was observed running the driver continuously for more than three days at 10 Gb/s, setting an upper bound of 10^{-15} on the BER; this measurement is schematically shown in Fig. 16.

C. Substrate Effect

The substrate connections were not connected to the V_{EE} 's (the lowest voltage of the circuit). All substrate connections were connected to a single pad at the bottom right of the chip as shown in Fig. 14. The reason the substrate was not connected to V_{EE} was to keep the current sources independent for testing purposes. The substrate pad was closer to the output pad Out+ as shown in Fig. 14.

This small lack of symmetry, which was the only unsymmetrical part of the layout, resulted in a discernible difference in the performance of the two differential outputs. As it can be seen in the eye diagram in Fig. 18, the output that is further away from the substrate pad is noisier than the other output. This signifies the importance of charge removal from substrates for circuits with very high currents.

IX. CONCLUSION

We have shown a novel BV-Doubler topology that can alleviate the low breakdown voltage of high-speed silicon devices for use in high-voltage drivers. This topology divides the output swing equally on two transistors allowing an output voltage swing of $2 \times BV_{\text{CER}}$ without exceeding BV_{CER} on any single transistor. This topology differs from the standard cascode by synchronously driving the base voltage of the upper transistor. The measured chip had a differential output swing of 8 V_{pp} at 10 Gb/s. A very conservative maximum value of V_{CE} was used in designing this circuit. As shown in [6], this process technology can sustain a V_{CE} swing as high as 3.2 V, and therefore, using the same process technology and design, one can achieve a differential voltage swing up to 12.8 V. One can, in principle, achieve even higher output swings by extending this idea, as mentioned in the last section, for output voltage swings as high as $3 \times BV_{\text{CER}}$ or even higher.

This chip consumed 3.7 W, which was very high, and many steps were taken to ensure the chip remained within operating temperature. After the chip was fabricated, it was noticed that the current in the base driving branch was unnecessarily high. Simulation showed that the same performance could have been achieved with at least 30% lower power consumption. A lower power consumption BV-Doubler based on this concept has been shown by Li and Tsai [17].

ACKNOWLEDGMENT

The authors would like to acknowledge IBM Corporation for chip fabrication. They would also like to thank B. Analui, J. Buckwalter, H. Hashemi, A. Komijani, and A. Natarajan for valuable technical discussion.

REFERENCES

- [1] H.-M. Rein and M. Moller, "Design considerations for very-high-speed Si-bipolar ICs operating up to 50 Gb/s," *IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1076–1090, Aug. 1996.
- [2] M. Reinhold, C. Dorschky, E. Rose, R. Püllela, P. Mayer, F. Kunz, Y. Baeyens, T. Link, and J. P. Mattia, "A fully integrated 40-Gb/s clock and data recovery IC with 1:4 DEMUX in SiGe technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1937–1945, Dec. 2001.
- [3] J. Müllrich, T. F. Meister, M. Rest, W. Bogner, A. Schöpflin, and H.-M. Rein, "40 Gbit/s transimpedance amplifier in SiGe bipolar technology for the receiver in optical-fiber TDM links," *Electron. Lett.*, vol. 34, pp. 452–453, Mar. 1998.
- [4] J. Hauenschild *et al.*, "A plastic packaged 10-Gb/s BiCMOS clock and data recovery 1:4-demultiplexer with external VCO," *IEEE J. Solid-State Circuits*, vol. 31, no. 12, pp. 2056–2059, Dec. 1996.
- [5] M. Meghelli, A. V. Rylyakov, and L. Shan, "50-Gb/s SiGe BiCMOS 4:1 multiplexer and 1:4 demultiplexer for serial communication systems," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1790–1794, Dec. 2002.
- [6] D. J. Friedman *et al.*, "SiGe BiCMOS integrated circuits for high-speed serial communication links," *IBM J. Res. & Dev.*, vol. 47, pp. 277–279, Mar./May 2003.
- [7] H.-M. Rein, R. Schmid, P. Weger, T. Smith, T. Herzog, and R. Lachner, "A versatile Si-bipolar driver circuit with high output voltage swing for external and direct laser modulation in 10 Gb/s optical-fiber links," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1014–1021, Sep. 1994.

- [8] Y. Yamauchi, K. Nagata, T. Makimura, O. Nakajima, H. Ito, and T. Ishibashi, "10 Gb/s monolithic optical modulator driver with high output voltage of 5 V using InGaP/GaAs HBTs," in *IEEE Gallium Arsenide Integrated Circuit (GaAs IC) Symp. Tech. Dig.*, 1994, pp. 207–210.
- [9] Z. Lao, M. Yu, V. Ho, K. Guinn, M. Xu, S. Lec, V. Radisic, and K. C. Wang, "High performance 10–12.5 Gbit/s modulator driver in InP SHTB technology," *Electron. Lett.*, vol. 39, no. 13, pp. 983–985, Jun. 26, 2003.
- [10] J. M. Carroll and C. F. Campbell, "A 14- v_{pp} 10 Gbit/s E/O modulator driver IC," in *IEEE Gallium Arsenide Integrated Circuit (GaAs IC) Symp. Tech. Dig.*, 2001, pp. 277–279.
- [11] J. Jeong and Y. Kwon, "10 Gb/s modulator driver IC with ultra high gain and compact size using composite lumped-distributed amplifier approach," in *IEEE Gallium Arsenide Integrated Circuit (GaAs IC) Conf. Tech. Dig.*, 2003, pp. 149–152.
- [12] R. Schmid, T. F. Meister, M. Rest, and H.-M. Rein, "40 Gbit/s EAM driver IC in SiGe bipolar technology," *Electron. Lett.*, vol. 34, no. 11, pp. 1095–1097, May 28, 1998.
- [13] —, "SiGe circuit with high output amplitude operating up to 23 Gb/s," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 886–891, Jun. 1999.
- [14] D.-U. Li, C. Tsai, and L.-R. Huang, "Laser/modulator driver with high modulation output operating up to 16 Gb/s using 0.35 μm SiGe BiCMOS process," in *Proc. IEEE Asia-Pacific Conf. Circuits Syst.*, Dec. , 2004, pp. 225–228.
- [15] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18- μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138–2146, Dec. 2003.
- [16] A. Kanda, Y. Umeda, and T. Enoki, "10 Gbit/s series-connected voltage-balancing pulse driver with direct-coupled current switches," *Electron. Lett.*, vol. 39, no. 12, pp. 908–909, Jun 2003.
- [17] D.-U. Li and C.-M. Tsai, "Efficient breakdown voltage doubler for 10 Gbit/s SiGe modulator drivers," *Electron. Lett.*, vol. 41, pp. 1095–1097, Feb. , 2005.
- [18] T. Sowlati and D. M. W. Leenaerts, "A 2.4 GHz 0.18 μm CMOS self-biased cascode power amplifier," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1318–1324, Aug. 2003.
- [19] D.-U. Li and C.-M. Tsai, "10–13.6 Gbit/s 0.18 μm CMOS modulator drivers with 8 v_{pp} differential output swing," *Electron. Lett.*, vol. 41, pp. 27–28, May , 2005.
- [20] A. J. Annema, G. Geelen, and P. de Jong, "5.5 V tolerant I/O in a 2.5 V 0.25 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 528–538, Mar. 2001.
- [21] B. Serneels, T. Piessens, M. Steyaert, and W. Dehaene, "A high-voltage output driver in a 2.5-V 0.25- μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 576–583, Mar. 2005.
- [22] S. Mandegar and A. Hajimiri, "A breakdown voltage doubler for high voltage swing drivers," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2004, pp. 103–106.
- [23] R. S. Muller and T. I. Kamins, *Device Electronics For Integrated Circuits*, 3rd ed. New York: Wiley, 2003.
- [24] G. W. Neudeck, *The Bipolar Junction Transistor*, 2nd ed. Reading, MA: Addison-Wesley, 1989.
- [25] M. Alioto and G. Palumbo, "CML and ECL: Optimized design and comparison," *IEEE Trans. Circuits Syst. I: Fundam. Theory Appl.*, vol. 46, no. 11, pp. 1330–1341, Nov. 1999.
- [26] K. M. Sharaf and M. I. Elmasry, "An accurate analytical propagation delay model for high-speed CML bipolar circuits," *IEEE J. Solid-State Circuits*, vol. 29, no. 1, pp. 31–45, Jan. 1994.
- [27] M. I. Elmasry, *Digital Bipolar Circuits*. New York: Wiley, 1983.



Sam Mandegar (S'03) received the B.S. degrees in electrical engineering and economics and the M.S. degree in electrical engineering from the California Institute of Technology (Caltech), Pasadena, in 2000 and 2003, respectively.

He is currently working toward the M.F.A. degree in film production at the University of Southern California, Los Angeles, and currently pursuing the doctorate in electrical engineering at Caltech. He is also a Design Engineer at Raytheon.



Ali Hajimiri (M'99) received the B.S. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1996 and 1998, respectively.

He was a Design Engineer with Philips Semiconductors, where he worked on a BiCMOS chipset for GSM and cellular units from 1993 to 1994. In 1995, he was with Sun Microsystems, where he worked on the UltraSPARC microprocessor's cache RAM design methodology. During the summer of 1997, he was with Lucent Technologies (Bell Labs), Murray Hill, NJ, where he investigated low-phase-noise integrated oscillators. In 1998, he joined the Faculty of the California Institute of Technology, Pasadena, where he is a Professor of Electrical Engineering and the Director of Microelectronics Laboratory. He is the author of *The Design of Low Noise Oscillators* (Kluwer, 1999) and holds several U.S. and European patents. His research interests are high-speed and RF integrated circuits.

Dr. Hajimiri is a member of the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC). He has also served as

an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), an Associate Editor of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS: PART II, a member of the Technical Program Committees of the International Conference on Computer Aided Design (ICCAD), Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and the Guest Editorial Board of Transactions of Institute of Electronics, Information and Communication Engineers of Japan (IEICE). He was selected to the top 100 innovators (TR100) list in 2004, and is a Fellow of Okawa Foundation. He is the recipient of Caltech's Graduate Students Council Teaching and Mentoring Award as well as Associated Students of Caltech Undergraduate Excellence in Teaching Award. He was the Gold medal winner of the National Physics Competition and the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, The Netherlands. He was a co-recipient of the JSSC Best Paper Award of 2004, the ISSCC Jack Kilby Outstanding Paper Award, two times co-recipient of CICC's best paper awards, and a three times winner of the IBM Faculty Partnership Award, as well as National Science Foundation CAREER Award.