A 24GHz, +14.5dBm Fully-Integrated Power Amplifier in 0.18μm CMOS

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Abstract

A 24GHz, +14.5dBm fully-integrated power amplifier with 50Ω input and output matching is fabricated using 0.18μm CMOS transistors. To enable this, a shielded-substrate coplanar waveguide transmission line structure is used to achieve low loss and small area. The power amplifier achieves a power gain of 7dB and a maximum single-ended output power of +14.5dBm with a 3dB bandwidth of 3.1GHz, while drawing 100mA from a 2.8V supply. The chip area is 1.26mm^2.

Introduction

The quest for multi-Gigabit wireless connectivity has fueled extensive research on higher frequency bands. The Industrial, Scientific and Medical (ISM) band at 24GHz is a promising candidate. Furthermore, an FCC ruling released in 2002 opened the 22GHz ~ 29GHz frequency band for ultra wideband (UWB) vehicular radar applications [1]. Consequently, research on 24GHz band wireless technologies has accelerated, demonstrating various building blocks for receivers in GaAs pHEMPT [2] and SiGe BiCMOS [3]-[4], as well as the introduction of a fully-integrated eight-path phased-array receiver [5] at this frequency.

While there have been some efforts on the receiver side, very little has been done to implement transmitter building blocks in low-cost CMOS processes. A CMOS power amplifier at 24GHz is among the most challenging building blocks to be implemented. To the best of our knowledge, the highest-frequency CMOS power amplifier reported to this date is a 0.18μm design at 8GHz [6].

Two main problems in a high-frequency fully-integrated power amplifier are the low unity power gain frequency, f_{max}, of MOS transistors, and the high-frequency loss of on-chip passive elements, such as inductors and transmission lines needed for impedance matching. For narrowband amplifiers where device capacitance is normally tuned out, f_{max} is the real metric for device speed. It is limited by resistive losses, primarily series gate resistance in MOSFETs. Generally, MOS transistors have lower f_T and f_{max} compared to SiGe bipolar transistors fabricated with the same feature size [7]. In the 0.18μm process used in this design, the NMOS transistors have an f_{max} of 65GHz that is a factor of two smaller than their SiGe bipolar counterparts.

Large substrate conductivity increases substrate-induced losses in inductor-based and coplanar waveguide-based impedance transformation networks. In a digital CMOS process this problem is exacerbated as transistor scaling constantly increases the substrate doping levels and substrate conductivity [8]. Moreover, at higher frequencies skin effect increases the ohmic losses of the inductors and transmission lines. This is due to the reduction of effective metal thickness which limits the benefits gained by using thicker metals. For example, the skin depth in Aluminum at 24GHz is about 0.5μm.

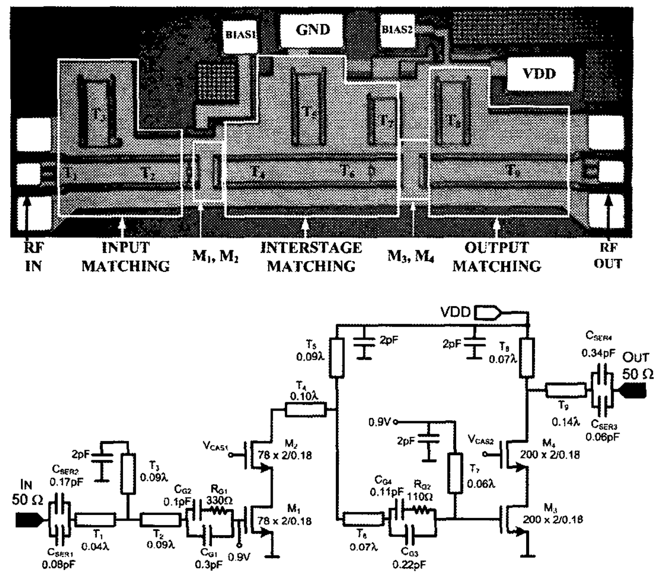

Fig. 1. Die micrograph and schematic of the 24GHz, 14.5dBm fully-integrated CMOS power amplifier, chip size: 0.7mm x 1.8mm.

In this design a shielded-substrate coplanar waveguide structure is used that effectively lowers substrate loss, reduces on-chip wavelength, and maintains symmetry of the two ground lines. This is an enhanced version of the slow-wave coplanar structure presented in [9]. This structure is used to make a fully-integrated CMOS power amplifier operating at 24GHz. The die micrograph of the fabricated amplifier is shown in Fig. 1. In the following section, we discuss the design process in more details.

Architecture and Circuit Design

This section describes the design evolution of the amplifier focusing on the methodology used for optimizing the matching networks. First, the substrate-shielded coplanar waveguide structure, an important element in the design of the 24GHz power amplifier shown in Fig. 1, is presented. Next, we discuss the amplifier stability and the design techniques used to achieve

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unconditional stability for all bias points. Finally, we discuss the techniques used to minimize the effect of the pad capacitances and variable wire-bond inductances.

A. Shielded-Substrate Coplanar Waveguide Structure

At 24GHz, large capacitive coupling to substrate lowers the quality factor of inductors. Therefore, inductance-based impedance matching networks will result in a large power loss. On the other hand, this frequency is not high enough for direct application of standard transmission lines due to their large length. For example, using a SiO_2 dielectric, on-chip λ at 24GHz is 6.3mm, therefore normal transmission-line based approaches for matching networks result in a long line length and thus significant power loss.

In normal coplanar waveguide structures made in CMOS processes with high substrate conductivity, capacitive coupling to the substrate is the dominant source of loss. On the other hand, in a microstrip structure with the same characteristic impedance, close proximity of the ground plane to the signal line demands a narrow signal line to maintain a reasonable impedance level. This effect increases metal ohmic losses and is aggravated by the skin effect. Fig. 2 shows the combination of the two structures in which the electric fields do not penetrate into substrate similar to a microstrip while the current and magnetic field distributions resemble that of a coplanar waveguide structure. This combination reduces both metal and substrate loss components.

The challenge in this structure is maintaining a high impedance level, while reducing the loss components. Slotting the bottom plate, as shown in Fig. 2, forces the return current to be mostly concentrated in the coplanar ground lines.

Compared to a microstrip line, larger separation between signal and return current in a coplanar structure stores more magnetic energy in space, resulting in a larger distributed inductance per unit length. To keep the characteristic impedance of the line constant, distributed capacitance of the line should be increased proportionately, to maintain a constant L to C ratio. This is done by widening the signal line which has the added advantage of reducing metal losses in the signal line. Larger distributed capacitance and inductance will also slow the wave. In this approach the relative permittivity of the TEM-mode wave can be as large as 20, which is five times greater than the relative permittivity of silicon oxide. This results in more than a factor of two reduction in the wavelength and hence the transmission line length, which will translate to lower passive loss.

B. Amplifier Design

The 24GHz power amplifier shown in Fig. 1 is a single-ended two-stage design that can directly feed a single-ended 50Ω antenna with no need for a Balun or a differential antenna. If a differential antenna is available, two amplifiers in parallel can produce 3dB higher output power similar to [10].

The stages are designed such that all the phase shifts needed for impedance matching are small, as shown in Fig. 1. This is done by proper choice of on-chip characteristic impedance and optimization of the matching network.

To minimize the effect of gate series resistance, R_G, which can be

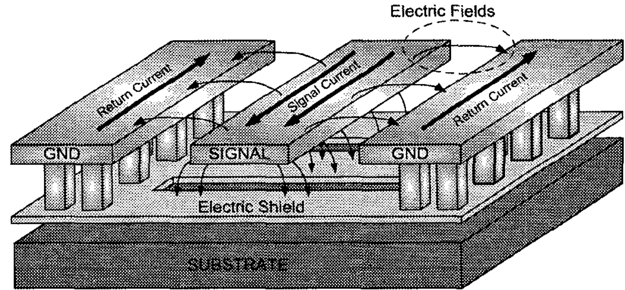

Fig. 2. Shielded-substrate coplanar waveguide structure.

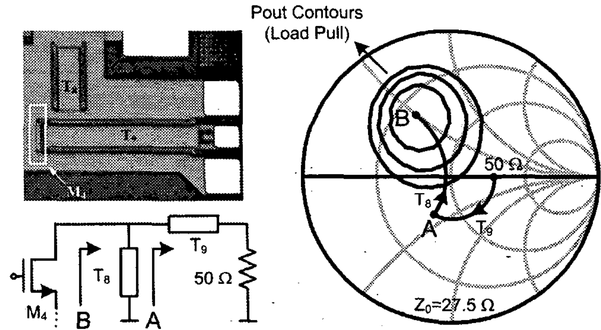

Fig. 3. Design of the output matching network; the smith chart reference impedance is the characteristic impedance of the transmission lines (27.5Ω).

the liming factor for f_{max}, the finger width of transistors was chosen to be 2μm with gate contacts at both ends. This also allows substrate contacts to be placed closer to the device, minimizing substrate losses.

The output stage matching is designed to convert the 50Ω antenna impedance to the proper impedance at the drain of M_4, maximizing output power and efficiency. As shown in Fig. 3, this proper impedance is chosen by the load pull simulation of the cascode pair while the gate of input transistor is driven by a large-signal source. T_8 acts as a shorted-stub inductor to resonate drain-substrate capacitance of M_4 while T_9 lowers the 50Ω antenna impedance for a higher output power. Inter-stage matching and input matching networks are designed based on the same principle.

For minimum passive loss, the output stage characteristic impedance should be lower than the inter-stage one, but to simplify the design and test procedures a single characteristic impedance of 27.5Ω was used for the transmission lines across the chip. A weighted least-mean-square (LMS) optimization with gradient-descent scheme was used to choose this characteristic impedance and all the transmission line lengths. All 2pF MIM capacitors used to short parallel stubs have a large width-to-length ratio to make the electrical length of the shorted stubs more accurate.

C. Cascode Transistor Pair and Stability of the Amplifier

In the CMOS process used, a single transistor biased for a maximum power gain in a common source configuration is not unconditionally stable at 24GHz. The cascode structure makes the device more unilateral and hence unconditionally stable. Also, a cascode pair has a higher drain-source breakdown

voltage, so a 2.8V supply can be used for 0.18μm devices that have a drain-source breakdown voltage of 2.5V.

The output stage cascode pair is shown in more detail in Fig. 4(a). The gate of M_4 is self-biased by R_2 and bypassed by C_1. While careful layout was carried out to minimize L_1, the parasitic series inductance of C_1, there remains a potential for high-frequency instability when L_1 is large. A simple analysis of the circuit is shown in Fig. 4(b). Neglecting gate-drain capacitance of M_4, the impedance looking into it's gate is:

$$Z_{IN} = \frac{1}{sC_2} + \frac{1}{sC_3} + \frac{g_m}{C_2 C_3 s^2} \quad (1)$$

For $s = j\omega$, this impedance has a negative real part equal to $-g_m/(C_2C_3\omega^2)$, indicating that the circuit could oscillate if there is a parasitic inductance between gate and ground. Series resistance R_1 is designed to make the circuit stable without reducing the amplifier gain at 24GHz. Using **(1)**, the condition for the stability can be expressed as:

$$R_1 > \frac{g_m}{C_2 C_3 \omega_{osc}^2} \quad (2)$$

$$\omega_{osc} = \frac{1}{\sqrt{L_1 C_{eq}}}, \quad C_{eq} = \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}\right)^{-1}$$

C_1 should be large enough to provide low impedance at the gate of M_4 while small enough to have a small series self-inductance.

In addition to the stability analysis discussed, some additional measures were taken to improve the low-frequency stability of the amplifier. In particular, C_{G1} and C_{G3} coupling capacitors were shunted with a series RC network designed to introduce resistive loss at low frequencies while maintaining the necessary dc block, as shown in Fig. 1.

The simulated Rollett stability factor [11], K, of the amplifier was greater than 30 for all frequencies between dc and 65GHz. This was done for all gate and drain biases. Special attention was paid to the large-signal stability of the amplifier. During measurements, there were no signs of oscillation under any bias condition, drive level, or wirebond inductance.

D. Other Issues

The amplifier is designed to accommodate a large change in the wirebond inductance. The change in inductance is caused by variations in the length and curvature of the wirebond. 3D electromagnetic simulations for the intended test board reveal a range of 0.2nH-0.5nH for the inductance, depending on different wirebond curvatures. Capacitors were placed in series with the input and output pads to resonate out this inductance, as shown in Fig. 1. Due to non-zero length of the transmission line between this capacitor and the wirebond, this approach does not completely eliminate the variable load impedance effect. Consequently, the matching network was modified to provide the same load impedance for the wirebond inductances and the series capacitance. In the large-inductance mode (wirebond inductance greater than 0.4nH), the voltage swing across the series

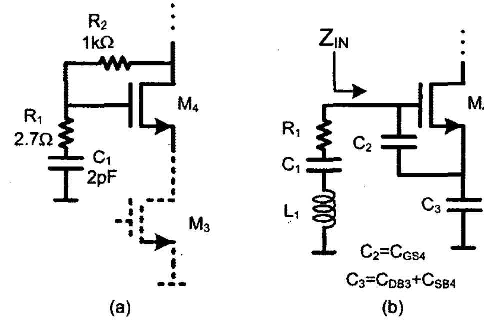

Fig. 4. (a) Self-bias of cascode transistor pair; (b) Equivalent circuit for the analysis of stability.

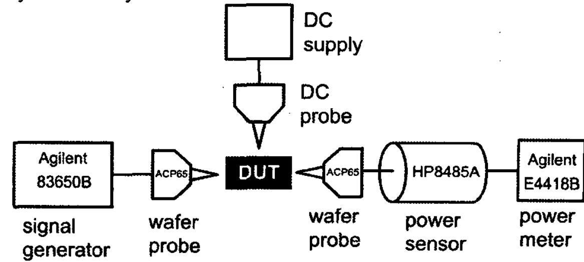

Fig. 5. Large-signal measurement setup.

capacitance can exceed the breakdown voltage of the MIM capacitors available in the process (~5V). A vertical parallel-plate (VPP) capacitor with a breakdown voltage in excess of 100V was designed and used to prevent capacitor breakdown [12]. The capacitance of the RF pads was absorbed into the transmission line structure by extending electric shield underneath the pads.

Experimental Results

The power amplifier was fabricated using 0.18μm CMOS transistors in a process with a substrate resistivity of 10Ω.cm. The chip occupies an area of 0.7mm x 1.8mm including pads. Quasi-3D simulations were performed on the complete structure as a part of the design cycle to verify amplifier's performance. In our measurement, the chip was attached to a gold-plated brass substrate using conductive epoxy to function as a heat sink and mechanical support.

Large-signal measurements were performed using the measurement setup shown in Fig. 5. The output is connected to a power meter with an Agilent HP8485A 26.5GHz power sensor. The sensor attenuates all harmonic signal power and therefore eliminates the need for a harmonic filter. All system power losses are calibrated out with a through measurement. As shown in Fig. 6, a single-ended output power of +14.5dBm at 24GHz was obtained with a small-signal gain of 7dB drawing 100mA from a 2.8V supply. The corresponding peak drain efficiency is 11%.

Small-signal measurements were also done using Agilent E8364A 50GHz network analyzer. TRL calibration was performed at the probe tips using CPW calibration standards on an Alumina substrate to measure the S-parameters of the amplifier, shown in Fig. 7. The 3dB bandwidth is 3.1GHz from 22.9GHz to 26GHz, while the peak gain is at 23.9GHz and the maximum S_{11} and S_{22}

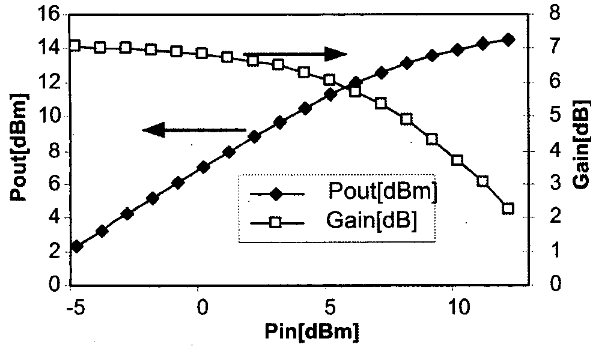

Fig. 6. Output power and amplifier gain vs. available input power using a 2.8V supply.

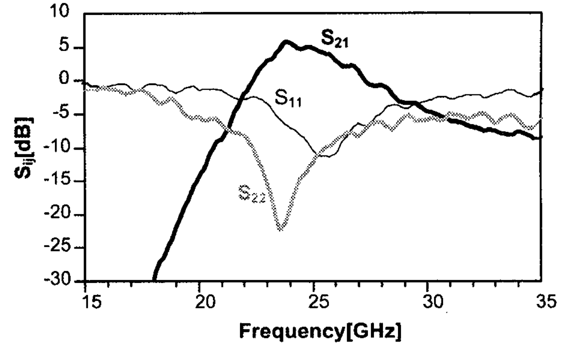

Fig. 7. Measured S-parameters of the amplifier, $V_{G1}= V_{G3}=1V$, $V_{DD}=2.8V$, and $I_{supply}=100mA$.

within the ISM band at 24GHz ~ 24.25GHz are -6.9dB and -16dB, respectively.

Fig. 8 shows the die photo of a substrate-shielded coplanar waveguide test structure fabricated in the same process. The top three metal layers were used for transmission line structure. An offset-overlapping second shield layer was added to shield the substrate at slots of the first one. Top metal layer is 4μm-thick Aluminum placed 11.7μm above substrate. Two shield layers use 1.25μm and 0.3μm thinner Copper metals placed 6.4μm and 2.2μm above substrate.

The test structure was designed for a target characteristic impedance of 27.5Ω, the same impedance used in power amplifier. Measurement results of the line are summarized in table I.

TABLE I
Measurement results of the transmission line at 24GHz

Parameter	Simulated	Measured
Attenuation constant (α)	0.5dB/mm	0.38dB/mm
Characteristic impedance (Z_0)	27.5Ω	28.9Ω
Relative permittivity (ε_r)	18.7	18.87

Conclusion

A shielded-substrate coplanar waveguide structure is designed which results in a low passive loss and small impedance transformation network area. The structure enables the design of a fully-integrated 24GHz power amplifier using 0.18μm MOSFETs which is three times higher than the fastest CMOS power amplifier reported to this date. This work shows that CMOS technology is a viable candidate for building fully-integrated transmitters at frequencies above 20GHz. A comparison of the power amplifier in this work and the previous work on high-frequency amplifiers (mostly in silicon) is summarized in Table II.

TABLE II
Comparison

Freq.	Device	P_{out}	Output	Ref.
24GHz	0.18μm CMOS	14.5dBm	Single-ended	This work
8GHz	0.18μm CMOS	22dBm	Single-ended	[6]
24GHz	0.18μm GaAs pHEMPT	18dBm	Single-ended	[2]
60GHz	0.13μm SiGe HBT	11.8dBm	Differential	[10]

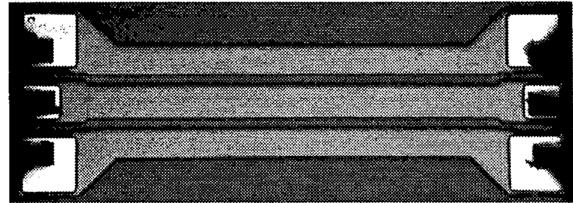

Fig. 8. Die photo of the test transmission line, signal line width is 60μm and gap is 24μm, size including pads: 1mm x 0.36mm.

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