Integrated Transversal Equalizers in High-Speed Fiber-Optic Systems

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***Abstract*—Intersymbol interference (ISI) caused by intermodal dispersion in multimode fibers is the major limiting factor in the achievable data rate or transmission distance in high-speed multimode fiber-optic links for local area networks applications. Compared with optical-domain and other electrical-domain dispersion compensation methods, equalization with transversal filters based on distributed circuit techniques presents a cost-effective and low-power solution. The design of integrated distributed transversal equalizers is described in detail with focus on delay lines and gain stages. This seven-tap distributed transversal equalizer prototype has been implemented in a commercial 0.18-μm SiGe BiCMOS process for 10-Gb/s multimode fiber-optic links. A seven-tap distributed transversal equalizer reduces the ISI of a 10-Gb/s signal after 800 m of 50-μm multimode fiber from 5 to 1.38 dB, and improves the bit-error rate from about 10^{-5} to less than 10^{-12}.**

***Index Terms*—Dispersion, distributed circuit, equalization, fiber-optic communications, transversal filter.**

I. Introduction

INTERSYMBOL interference (ISI) is a fundamental problem in digital communications in bandwidth-limited links. One such example are multimode fibers, which are the dominant fiber type in LAN links (Gigabit Ethernet [1], Fiber Channel [2]). In these links, the ISI is the dominant power penalty in the link power budget and effectively sets the limits for the achievable data rate or transmission distance.

The main source of ISI in a fiber-optic system is signal pulse broadening due to fiber dispersion. There are three types of dispersion in a fiber-optic system: modal dispersion, chromatic dispersion, and polarization mode dispersion [3]. In a multimode fiber, different mode groups have different velocities, which is called modal dispersion. Chromatic dispersion is due to the fact that different wavelengths of light have different velocities. The polarization-mode dispersion, which comes from different velocities of different polarizations, can be neglected in multimode fibers.

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In multimode fiber-optic links, for a given data rate, the ISI effectively sets the limit on the achievable link distance, due to the fact that it increases exponentially with the distance and thus, dominates the other penalties in the link power budget. For example, Table I shows the effective bandwidth and achievable link distance in 10 GBASE-S base links in the IEEE 802.3ae standard, running at 10.3125 Gb/s. It is evident that neither the common FDDI-grade 62.5-μm multi-mode fiber (MMF) nor 50-μm MMF is capable of achieving practical distances. Even though the latest laser-optimized 50-μm next-generation MMF (NGMMF) can achieve the same distance as in the previous generation networks (300 m), any further increase in the data rate would imply shorter distances. Furthermore, there is a need to utilize the huge installed base of multimode fibers.

In order to reduce the dispersion effect, different methods have been proposed and implemented in all three parts of a regenerator span (transmitter, fiber, and receiver), and in both optical and electrical domains [4]–[6]. The main criteria for a good dispersion reduction method are small power penalty (low loss), good integration with current networks, low cost, and adaptability. The latter is important because: 1) dispersion is usually time varying due to environmental change such as temperature variation and 2) dispersion is also related to fiber length, and thus, an adaptable solution would be faster, easier, and cheaper to implement and maintain.

In the electrical domain, fiber dispersion can be compensated at the transmitter by pre-emphasis [7] or coding [8]. However, both approaches lack adaptability. Instead, equalization at the receiver is preferred, which is expected to be integrated with the receiver circuit. Therefore, there is a strong demand for an integrated equalizer solution in high-speed fiber-optic communications, especially in cost-sensitive short-haul systems.

This paper is organized as follows. Section II presents the distributed transversal equalizer, with comparison to other transversal equalizer implementations. Section III describes the design of delay elements and gain stages. Measurement results of prototypes are presented in Section IV. Conclusions are drawn in Section V.

II. Distributed Transversal Equalizer

A. Transversal Equalizer

In a communication system, equalization is the process of correcting channel induced distortion. In a multimode fiber-optic channel, modal dispersion is the main source of this distortion [9]. An equalizer is a filter that can be adjusted

TABLE I
ACHIEVABLE DISTANCES IN 10-Gb/s ETHERNET LINKS USING VARIOUS TYPES OF MULTIMODE FIBERS

Fiber @ 850nm Wavelength	Fiber Modal Bandwidth (MHz·km)	Achievable Distance at 10Gb/s (m)
62.5 μm MMF	160	26
50 μm MMF	500	82
50 μm NGMMF	2000	300

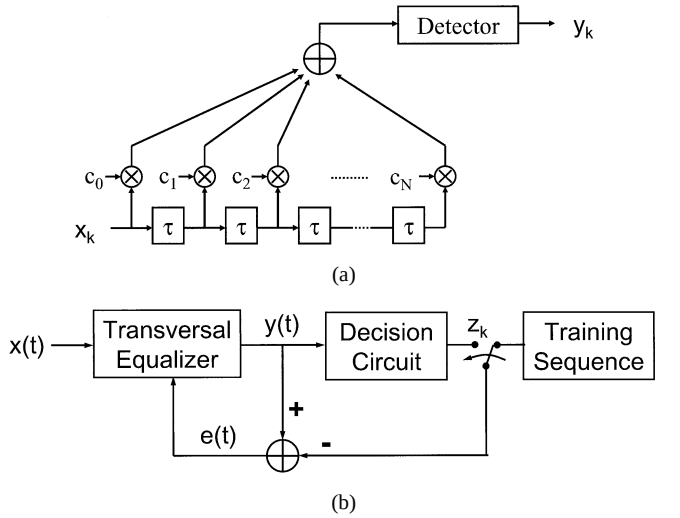

Fig. 1. Transversal equalizer. (a) Transversal filter. (b) Adaptive transversal equalizer.

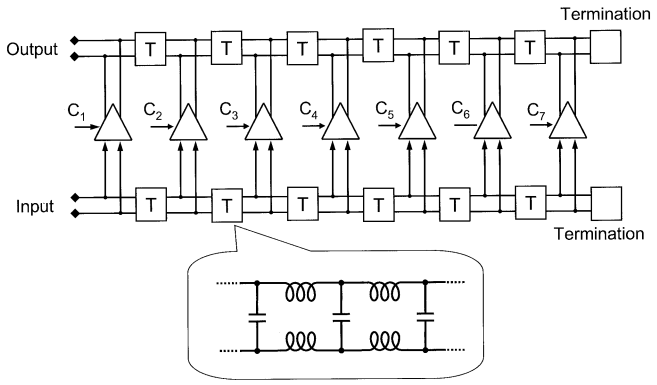

Fig. 2. Schematic of prototype equalizers.

to compensate for the distortion of the channel. Equalizers have been widely used in telephone networks and magnetic recording systems [10]. Transversal filter equalizers are of particular interest. They have relatively simple structures, can compensate many types of linear distortion, and can be made adaptive with simple algorithms. They can also be used as building blocks for more advanced equalizer architectures, such as a decision-feedback equalizer [11], [12] and maximum likelihood detection [13].

In a transversal equalizer [Fig. 1(a)], the input signal $x(t)$ propagates along a delay line. The signal $x(t)$ and its delayed versions $x(t-k\tau)$ (where $\tau = T$, the signal period, and $k = 1, \ldots, n$) are *tapped* along the delay line, multiplied by equalization coefficients (weights), and then summed to generate the equalized output $y(t)$. Thus, this architecture is sometimes referred to as a *tapped-delay-line* structure. A fractionally spaced equalizer (FSE), in which each tap has a delay of $\tau < T$, can reduce the aliasing problem in a T-spaced transversal equalizer and improve the equalizer performance [14].

One implementation of an adaptive transversal equalizer is shown in Fig. 1(b). In the initial training period, a known training sequence is transmitted and compared with its local copy in the receiver to find the channel characteristics and calculate the initial values for the equalization coefficients. Then the coefficients can be adjusted based on the decision results using an adaptive algorithm such as least mean square (LMS) [15] or zero-forcing algorithm [16]. Other implementations (blind equalization) exist, in which no training sequence is used.

At low speed, transversal equalizers can be implemented as digital finite-impulse response (FIR) filters: the input signal is first sampled and digitized, and the delay line can be constructed using a shift register [17] or memory [18]. The maximum data rate of digital FIR filters is limited by the speed of the digitizer and the power consumption and circuit complexity required for the high-speed implementation. In addition, clock generation poses another problem if fractionally spaced equalization is required.

Continuous-time transversal equalizers have been explored for high-speed applications, using charge-coupled devices (CCDs) [19] and surface accoustic wave (SAW) filters [20], as well as switch capacitors [21] and G_m-C ladder filters [22], [23]. Besides speed, such analog equalization has an additional advantage: Since sampling is done after equalization, signal delay in the equalizer does not affect the performance and stability of the clock-and-data-recovery (CDR) timing loop [24]. However, as signal speed further increases beyond 1 Gb/s, even these analog equalizers become inadequate to achieve the high-speed operation. We try to address this problem by using RF/microwave techniques.

B. Distributed Architecture

Distributed circuits are a good candidate for high-speed integrated circuits because of their unique wideband characteristic, which was originated from traveling-wave amplifiers [25], [26]. Fig. 2 shows an integrated transversal filter with a distributed architecture. The similarity with a traveling-wave amplifier is immediately evident. In fact, it can be viewed as a distributed amplifier operating in the reverse-gain mode. The input signal travels along the input transmission lines, and is tapped by each gain stage in sequence (from left to right in Fig. 2). Thus, the loaded transmission lines act as delay elements. The tapped signal is amplified by each gain stage by a gain proportional to the corresponding equalization coefficient (weight), and the output signals from all stages are added on the output transmission lines. It should be noted that the delay between adjacent

stages consists of that from both the input and output transmission lines.

Compared with conventional digital and analog transversal equalizer architectures, this architecture has the following advantages.

- It is an RF implementation, which can operate at very high data rates compatible with all current fiber-optic systems.
- It is an integrated circuit solution, which reduces the system complexity and cost significantly compared with conventional optical methods.
- The equalization coefficients can be realized by the gain from each stage, and thus, it is inherently adaptive.
- It is more power efficient since there is no power-hungry DSP as in digital implementations.
- Fractionally spaced equalization can be easily implemented without oversampling.

This architecture was first contemplated by Rauscher [27]. In 1989, Schindler developed an MMIC band-pass transversal filter at 9.8–11.1 GHz using microstrip lines and on-chip capacitors [28]. Kasper and Mizuhara first suggested the use of an integrated transversal filter for fiber-optic equalization [4], followed by others with simulation results [29], [30]. In 1997, Jamani *et al.* [31] and Borjak *et al.* [30] reported the first implementations using reverse-gain mode and forward-gain mode (in traveling-wave amplifier terminology), respectively. The latter group later switched to the reverse-gain mode architecture [32]. In 2000, Lee and Freundorfer introduced the Gilbert cell to generate both positive and negative weights [33]. These implementations verified that it is feasible to use distributed amplification techniques to achieve integrated transversal equalizer for high-speed fiber-optic systems.

However, there are important questions to be answered and problems to be solved.

- Analog weight adjustment is needed. There is no such mechanism reported in [30] and [32], and only binary weight control (on/off) in [31] (because of the cascode gain stage) and [33]. Without analog weight adjustment, adaptivity cannot be achieved.
- Unlike a traveling-wave amplifier, the gain stages have to be controlled independently with varying weights to achieve the adaptive transfer function. This makes it very difficult to maintain the same loading on the transmission lines from all stages at all time, i.e., the transfer function itself tends to disrupt the distributed circuit characteristics.
- Systematic analysis and equalization test data are still lacking.

III. Design

It is the goal of this work to answer the questions above in the context of a practical fiber-optic system [34]. A generic 10-Gb/s multimode fiber-optic link was chosen, which is fully compatible with the newly adopted 10 Gigabit Ethernet standard (IEEE 802.3ae) [1]. Based on system simulations using data from different lasers, fibers, and launch conditions, link distance improvement and failure rate was evaluated versus complexity, number of stages, and delay per stage. It was concluded that a seven-tap transversal equalizer with a 50-ps delay per stage would be adequate [35].

A. Delay Lines

As in any distributed circuit, the design of transmission lines is of critical importance [36]. In the case of distributed transversal equalizers, an additional constraint is the large time delay per stage. For the prototypes, the delay per stage is specified as 50 ps, i.e., half of the symbol period. Microstrip lines or coplanar waveguides would be too long to effectively implement this delay on chip. For example, for microstrip lines with metal groundplane, the phase velocity of a transverse electromagnetic (TEM) wave can be estimated as $v = c/\sqrt{\epsilon_{\mathrm{SiO_2}}} = 0.5c$, and then the microstrip line length per stage would be $l \approx vt_d = 0.5c \times 50$ ps $= 7.5$ mm. Even if the loading effect is taken into account, the required length is still impractical. The total length of delay lines is a function of the number of bits of ISI that the filter is intended to cancel. Therefore, the physical size limitation still exists even when using smaller τ for each stage, which results in a larger number of stages. Considering these practical constraints, the delay elements were implemented using artificial transmission lines constructed with *LC* ladders of spiral inductors and MIM capacitors. For a given chip area, this approach can generate a larger time delay.

The inset in Fig. 2 shows a section of the transmission line structure. Since the spiral inductors are densely packed, the electromagnetic coupling between them has to be properly modeled. A six-port electromagnetic simulation [37] is used to simulate the whole transmission line section, and generate frequency-swept S-parameters for circuit simulation.

Another important design consideration is the ac ground path. Since the physical size of the equalizer is comparable to the wavelength of the signal, it is critical to have a well-defined return path for the ac current. This is a difficult problem for a wideband circuit like the equalizer, particularly because of the lossy and poorly modeled silicon substrate. In our design, this is addressed by adopting a differential architecture for the equalizer, i.e., using differential delay line structures and differential gain stages. This ensures a local virtual ground within each gain stage and each section of delay line structures, since the fundamental frequency components of the differential ac currents cancel each other. The differential architecture also reduces the return-path loss significantly.

B. Gain Stage

The function of the gain stage in a transversal filter is to implement the equalization coefficient (weight). The gain stage should have a flat and linearly controllable amplitude response. It should also be able to change the phase of its gain by 180° in order to generate negative coefficients. A flat group-delay response across the equalizer bandwidth is required to prevent phase distortion in the equalization process. This is critical, since such phase distortion cannot be easily compensated by equalization itself. Therefore, the gain stage can be considered an analog multiplier with a high-speed data input and a low-speed control signal. In addition, the gain stage should present a constant load to both the input and output

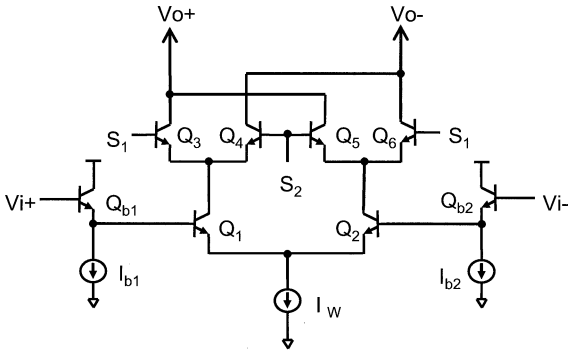

Fig. 3. Gain stage.

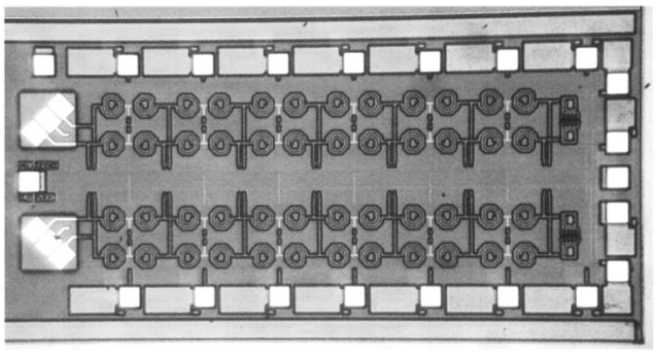

Fig. 4. Seven-tap prototype transversal equalizer.

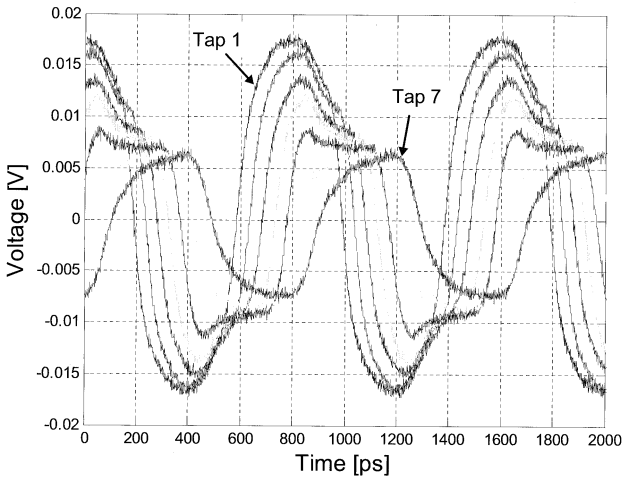

Fig. 5. Tap-delay uniformity measurement using 2.5-Gb/s square signal. We observe uniform tap delays, with typical values of approximately 45 ps.

transmission lines when changing the weights, in order to maintain a constant delay between adjacent stages.

Fig. 3 shows the simplified schematic of the gain stage. The core of the circuit is a Gilbert cell (Q_1–Q_6). The absolute value of the weight is implemented using the tail current source I_w. In this manner, the linearity of the weighting function, i.e., between I_w and the output voltage, is better than a cascode structure as in [31]. The sign of the weight is implemented using two differential pairs (Q_3, Q_4, Q_5, Q_6) to steer the differential current from Q_1 and Q_2 to the output transmission lines. The control signals of these transistors (S_1 and S_2) are analog voltages ($V_{\rm on}$ and $V_{\rm off}$) selected by a single digital bit S, which represents the sign of the corresponding weight. Because the output nodes are always connected to the collector of an ON transistor and that of an OFF transistor, there is no variation in the loading of the output transmission lines when the sign of the coefficient is switched.

The differential input signals are buffered using emitter followers (Q_{b1}, Q_{b2}, I_{b1}, I_{b2}). Buffering reduces the loading and thus, improves the linearity of the phase response on the input transmission lines. Further, the buffers are biased with constant currents, and thus, the parasitic capacitances of Q_{b1} and Q_{b2} do not change with the applied weight (I_w). Hence, there is no variation in the loading of the input transmission lines.

The gain stage satisfies the *strong impedance mismatching* condition [38] between succeeding stages (the input delay lines, emitter-follower buffers, core differential amplifier, switch pairs, and output delay lines), and therefore, can achieve the stringent requirements for bandwidth and group delay.

C. Prototypes

A seven-tap prototype of distributed transversal equalizers was designed and fabricated [34] using a 0.18-μm SiGe BiCMOS process with f_T of 120 GHz [39]. Fig. 2 shows its top-level schematic. The filter was simulated using ADS [40] with frequency-swept S-parameters of the delay lines that were obtained from EM simulations.

Fig. 4 shows the chip micrograph of the prototype transversal equalizer. It occupies an area of 3 mm $\times$ 1.5 mm, including pads. The pads on the top are inputs of sign bits of weights, and the bottom ones are inputs of absolute values of weights (reference voltage for the current mirror). The pads on the right are for ON/OFF voltages and dc bias. The pads on the left are for differential input and output, and are tilted 45° for RF probing. Note that the terminations are implemented with multiple resistors in parallel, which can be laser trimmed to fine tune the matching properties of the transmission lines.

IV. Measurement Results

Fig. 5 shows the step response of the equalizer to a 2.5-GHz square-wave input with each tap weighted independently. The delay per stage is approximately 50 ps. The earlier taps demonstrate more peaking and less attenuation than the later stages.

Fig. 6 shows the frequency response of four stages of the equalizer with each tap weighted independently. Consistent with the time domain measurement, the earlier taps show more peaking and less attenuation. In particular, tap 5 demonstrated a smooth response that peaked in the 3–6-GHz band. Not surprisingly, tap 5 had the highest weighting factor in the most successful data transmission measurements described below. The amplitude fluctuation is larger than the simulation, possibly due to the following reasons: 1) the measurement was single-ended instead of differential, i.e., only one input and one output were used; 2) the termination was not fine tuned to achieve the best matching for both transmission lines; and 3) the wideband modeling of transistors and spiral inductors was not accurate.

The ability of the circuit to equalize highly dispersed data signals was tested using the setup in Fig. 7, which is similar to its application environment. A pattern generator was used to drive an 850-nm vertical cavity surface emitting laser (VCSEL) using

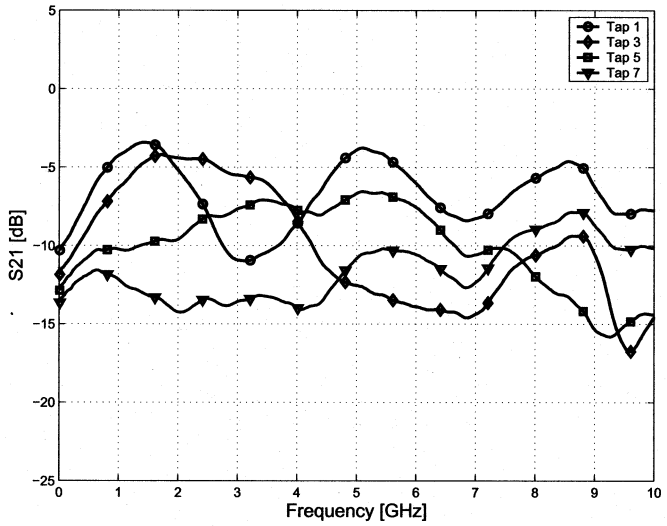

Fig. 6. Measured $S_{2,1}$ data for taps 1, 3, 5, and 7.

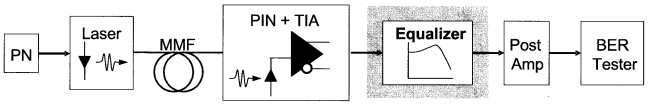

Fig. 7. Typical equalized link diagram. The equalizer is placed after the transimpedance amplifier (TIA) and before the postamplifer, and is not present in Ethernet and Fiber Channel links.

direct modulation, and 800 m of 50-μm noncompliant next-generation MMF fiber was used to generate distortion on the signal. The fiber was noncompliant because it did not meet any of the six masks in the specifications [41]. The pattern was a $2^{31}-1$ pseudorandom bit sequence (PRBS) pattern and the data rate was 10 Gb/s. This generated a signal with 5 dB of ISI and 62 ps of deterministic jitter (DJ) at the input of the equalizer.

The response of each tap individually was measured for different values of the tap coefficient, and an optimization routine was used to fit a linear combination of the individual signals to an idealized output with a raised cosine output characteristic. Rigorous linearity measurements were performed to validate this procedure. After each tap coefficient and sign was determined, the coefficients were fine tuned by hand while monitoring the eye diagram and the bit-error rate (BER) to determine the optimum set point. As shown in Fig. 8, the equalized signal has residual ISI of only 1.38 dB and a DJ of only 38 ps. The overall BER was improved from about 10^{-5} to less than 10^{-12}. The total power dissipation, including all biasing circuits, was 30 mW, plus 2 mW per active coefficient (typical dissipation is 40 mW).

The equalization chip was designed to operate on 10-Gb/s signals. To explore its limits, we tested it at 14 Gb/s (limited by test equipment). The signal from the pattern generator passed through the same setup as before, resulting in even larger eye closure (11 dB). Similar to the previous case at 10 Gb/s, the equalizer reduced the ISI penalty to 2.2 dB and reduced the deterministic jitter from 60 to 21 ps.

V. Conclusion

Integrated transversal equalizers based on distributed circuit techniques have been introduced as the solution for dispersion compensation in high-speed fiber-optic communications. The dispersion problem and compensation techniques were discussed, with the emphasis on adaptive equalization and its implementations. The design of integrated transversal equalizers has been further described with detailed analysis on delay lines and gain stages, followed by measurement results for a seven-tap 10-Gb/s prototype. Future work will focus on the other part of the challenge: How to generate the equalization coefficients at such high speed and make the equalizer fully adaptive.

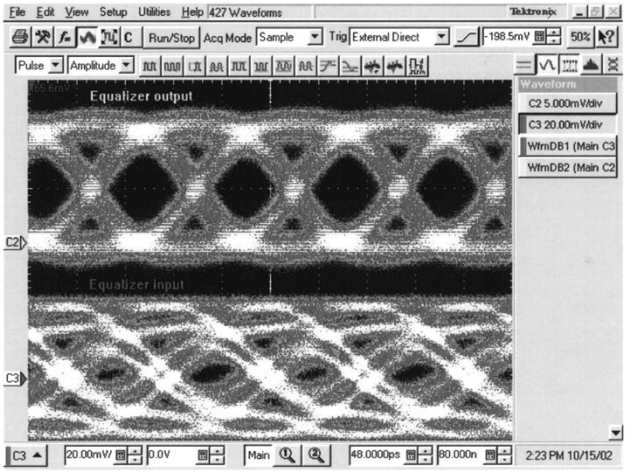

Fig. 8. Eye diagrams for 800-m 50-μm of multimode fiber before and after equalization.

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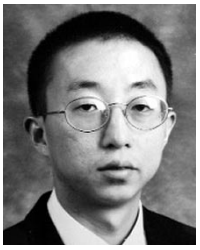

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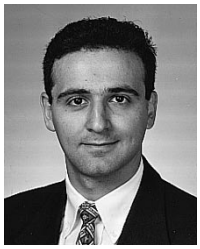
Dr. Kash is a Fellow of the American Physical Society.



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Dr. Hajimiri was the Bronze Medal winner of the 21st International Physics Olympiad, Groningen, the Netherlands, and the Gold Medal winner of the National Physics Olympiad. He was a corecipient of the IEEE International Solid-State Circuits Conference 1998 Jack Kilby Outstanding Paper Award and the winner of the IBM faculty partnership award. He is an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS: PART II and a Member of the Technical Program Committee of the IEEE International Solid-State Circuits Conference (ISSCC). He has also served as Guest Editor of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES and on the Guest Editorial Board of the *Transactions* of the Institute of Electronics, Information and Communication Engineers of Japan (IEICE).