An Active Analog Delay and the Delay Reference Loop

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***Abstract* — Wireline signal processing circuits such as transversal equalizers rely on true time delay. An active analog delay stage is proposed that requires a sixteenth of the area of a comparable LC delay line. A delay reference loop is also presented to tune the delay stage against process, voltage, and temperature variations. A reference signal is introduced to tune the delay. The impact of non-idealities must be considered to understand the relationship between the reference frequency and the locked time delay. A SiGe BiCMOS implementation of the active analog delay stage and delay reference loop is presented that operates to 10Gb/s.**

***Index Terms* — delay reference loop, delay locked loop, true time delay, analog delay, equalization, tapped-delay lines**

I. Introduction

Optical fiber and copper backplane cannot be treated as ideal channels in multi-gigabit-per-second wireline communication. Dispersion in fiber or copper interconnects drastically reduces system sensitivity. To reach higher bit rates or extend transmission distance, transceivers require channel equalization.

Transversal filters have been suggested for equalization of linear impairments at high frequencies [1]. A transversal filter, shown in Fig. 1, is constructed from the weighted sum of a tapped-delay line. The transversal filter becomes an equalizer when the output signal is monitored to adjust the weights, c_k. This paper addresses the implementation of time delay in an integrated circuit at 10Gb/s.

Time delay can be realized through transmission lines, lumped LC delay lines [2], or active devices [3]. Transmission line implementations often require an excessive chip area. At 10Gb/s, a single period delay is about one centimeter long. Lumped LC delay lines are also area-inefficient because of the required inductance values. Losses along both transmission lines and LC lines prevent cascading too many stages. Furthermore, the power consumption is large because of the low impedance of the lines.

In digital applications, delay is realized by reducing the bandwidth of a switching stage. The subsequent switching of an unloaded stage restores the rise time of the digital waveform [4]. This approach is not useful in analog applications that are sensitive to signal distortion. The active analog delay stage should demonstrate constant bandwidth at a variety of delay values.

Accurate delay requires robustness to process, voltage, and temperature (PVT) variations. Proper delay tuning is achieved with a delay reference loop (DRL). The DRL employs a reference frequency to stabilize the time delay. This reference frequency might come from an off-chip source or the locally regenerated clock in the case of an equalizer. As opposed to delay-locked loops that shift the delay to align an unknown signal, the DRL adjusts the delay to a given reference tone. However, the relationship between the locked delay and the reference frequency is influenced by circuit non-idealities.

II. Active Analog Delay

An active delay should conserve area without requiring excessive power consumption. The equalizer can compensate some distortion created by the tranversal filter provided the delay stage has a reasonably flat group delay.

True time delay is represented in the Laplace domain as e^{-sT}. While the pole-zero representation of this function is infinite, the first-order approximation is

$$e^{-sT} \sim \frac{1 - sT/2}{1 + sT/2}. \tag{1}$$

Equation (1) can be synthesized using the common-emitter stage (differential pair) depicted in Fig. 2. Ignoring the second pole associated with C_π, the all-pass transfer function of the delay stage is

$$A(s) = \frac{g_m R_c}{1 + g_m R_e} \cdot \frac{1 - sC_t(1 + g_m R_e)/g_m}{1 + sC_t R_c}. \tag{2}$$

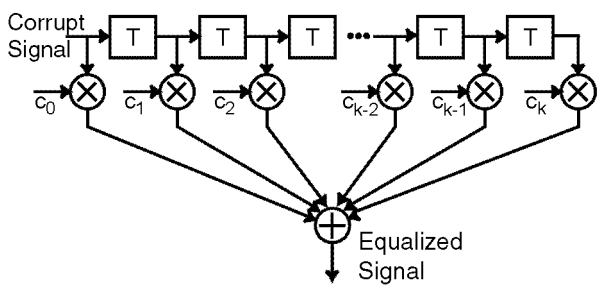

Fig. 1. Transversal Filter for Equalization

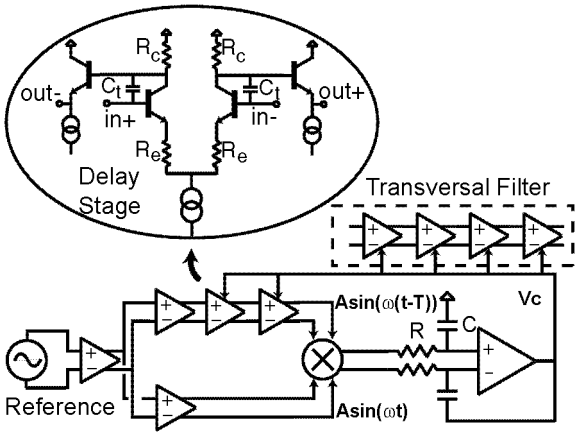

Fig. 2. The delay reference loop topology and the proposed active analog delay.

where g_m is the transconductance, R_c and R_e are the collector and emitter resistances, and C_t is the total capacitance between the base and the collector. This capacitance is often referred to as the Miller capacitance because the gain of the stage enhances its impact on the dominant pole of the stage. Emitter degeneration improves the dynamic range and the bandwidth of each delay stage, which is particularly important in cascading stages.

In (2), the left-half plane pole and the right-half plane zero should have the same absolute frequencies, *i.e.*

$$\frac{g_m R_c}{1 + g_m R_e} = 1, \tag{3}$$

resulting in a unity low frequency gain. This condition also prevents severe attenuation or saturation when cascading stages and alleviates the Miller capacitance. The time delay of the stage, *T*, is controlled by the frequency of the pole (and zero). Since both frequencies are proportional to C_t, the stage delay is controlled with a variable capacitance. The placement of a tuning capacitor, C_t, magnifies the inherent device capacitance, C_μ, without restricting the bandwidth because the pole and zero move in tandem. The required capacitance is on the order of $g_m T/2$. A stage time-delay of half of a bit period is usually chosen for equalization applications. Since g_m is on the order of tens of millisiemens for typical current levels, the required capacitance is less than a picofarad and is, thus, area efficient.

If we include the impact of C_π, there is another pole located close to the f_T of the transistors. However, C_t can impact the transistor speed if it dominates C_π. The transistor speed is approximately

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_t + C_\pi}. \tag{4}$$

Clearly, if C_t dominates C_π the f_T decreases at the same rate that the time delay increases and

$$f_T \cdot T \cong \frac{1}{2\pi}\frac{g_m}{C_t} \cdot \frac{2C_t}{g_m} = \frac{1}{\pi} \tag{5}$$

Therefore, the amount of delay variation per stage is limited. The useful delay variation range is restricted by C_π.

III. Delay Reference Loop

Implementing any delay in an integrated technology compels consideration of the process, voltage, and temperature (PVT) variations. We use a delay reference loop (DRL) to compensate for these PVT variations, as shown in Fig. 2. The DRL implementation is general to any tunable delay lines whether active or passive. As opposed to delay locked loop (DLL) topologies that aid clock recovery and frequency synthesis, the DRL generates an accurate time delay with a reference tone frequency.

The feedback dynamics with a conventional multiplier as a phase detector ensure that the stable equilibrium point is in quadrature to force the error voltage to be zero.

For a general loop filter, $H(s)$, the steady-state satisfies

$$\phi = \omega G H(s) \cos\phi \tag{6}$$

where $\phi = \omega T$ and G is the open loop gain, the product of the multiplier gain, the time delay control gain, and the reference signal amplitude. To reach the quadrature condition, the term on the left side must be zero at dc. This can be achieved with an integrator, $H(s) = 1/s$.

Often we are forced to consider non-idealities. With an imperfect integrator with finite gain, A_v, of the feedback

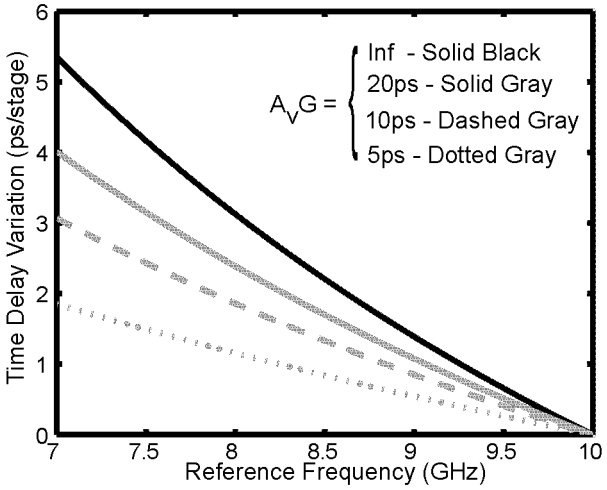

Fig. 3. Range of time delay variation for different total gain. The effect of the imperfect integration is reduced variation.

operational amplifier, the loop filter transfer function is $H(s) = A_v/[1 + sRC(1 + A_v)]$, where R and C are the resistance and capacitance of the loop filter.

Equilibrium points of the imperfect integration satisfy the equation:

$$T = A_v G \cos \omega T \tag{7}$$

If A_v is infinite, (7) reduces to $\cos(\omega T) = 0$ and the stable locked state is a delay of one fourth the reference period. Otherwise, (7) can be solved numerically for a unique equilibrium time delay. Fig. 3 demonstrates that non-ideal gain cuts down on the achievable delay variation per stage. Nevertheless, the choice of total gain, $A_v G$, seems arbitrary since there is a unique mapping between the reference frequency and the resulting time delay. In fact, only the range of time delay is determined by the gain. Hence, the gain is chosen to achieve the delay variation desired of each delay stage over a particular frequency range.

IV. Experimental Results

The circuit was implemented in a SiGe BiCMOS process. We chose an ECL compatible voltage swing of 300mVpp. For the delay stage, the collector resistance is 150Ω and, therefore, the emitter resistance that achieves unity gain through degeneration is 120Ω. A series combination of a varactor and large MIM coupling capacitor are placed between the base and collector to isolate the control voltage. If the MIM capacitance is large enough, the varactor dominates the series capacitance. The varactor was implemented using a reverse biased junction diode. This device was favored over a MOS accumulation mode varactor because of the smoother C-V relationship.

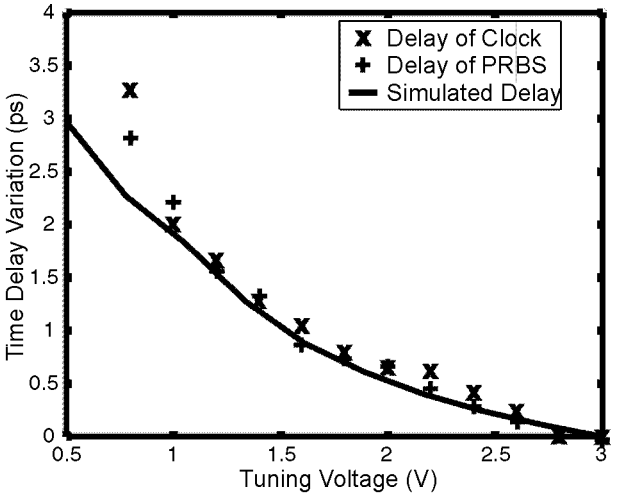

Fig. 4. Comparison of the simulated and measured open-loop time delay per stage.

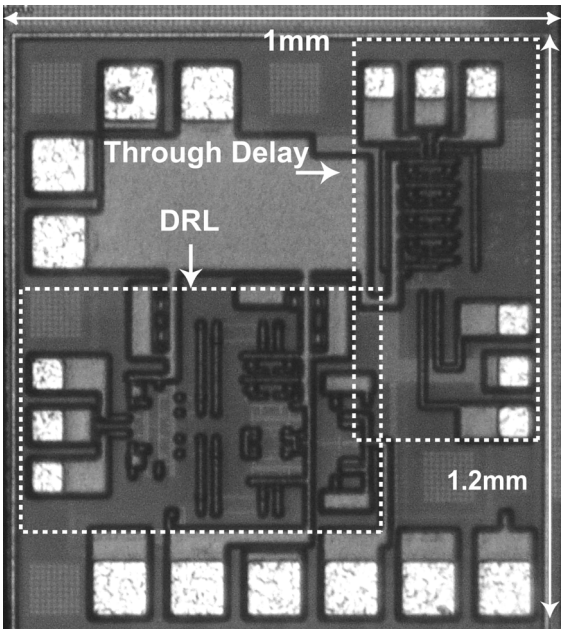

Fig. 5. Chip microphotograph of active analog delay line and delay reference loop.

The simulated bandwidth of the delay stage varied by less than 10% for a 25% change in delay, *i.e.*, the bandwidth of the delay varies between 27 and 30GHz while providing tuning of over 3ps per stage for nominal stage delay of 12.5ps. The tuning range was chosen to allow locking over PVT variations. However, larger ranges might be used to operate at different data rates.

The total area of a single 12.5ps delay stage is 0.0055mm^2. For comparison, the passive LC delays of [2] requires 0.35mm^2 per stage to provide 50ps of delay. The passive LC delay occupies 16 times the area per delay than the active stage.

The measured time delay for the active analog delay stage is compared with Spectre simulations in Fig. 4. The DRL is shut down and the control voltage is scanned. Both clock and PRBS are used because the PRBS does not have any spectral content at the clock frequency. The agreement for both a clock and the PRBS sequence at 5Gb/s implies that the group delay is relatively flat. The simulation results demonstrate close agreement until the control voltage falls below 1V. At this point, the bias of the varactor is no longer strictly reverse since the swing of the stage brings the base voltage above the control voltage. Hence, the electron drift in the junction is impaired by the shift from the reverse to forward bias condition and the capacitance increases.

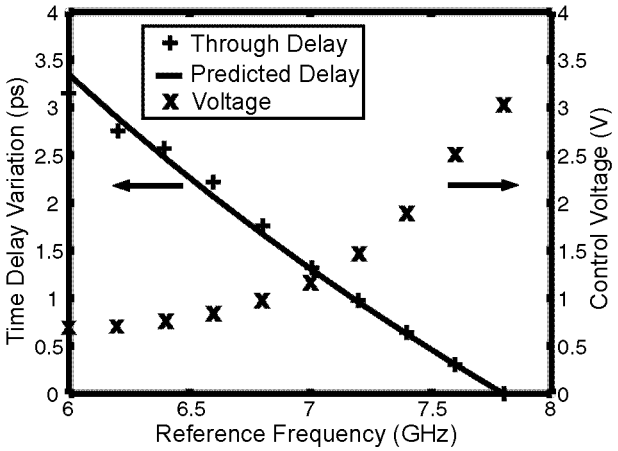

Fig. 6. Comparison of the predicted and measured time delay variation at difference reference frequencies.

The delay reference loop consists of a symmetric Gilbert multiplier phase detector with gain of 95mV/rad. A differential operational amplifier is configured as an inverting integrator and has bandwidth of 1kHz. A chip microphotograph is provided in Fig. 5. The circuit includes a separate through delay path, tuned from the DRL circuit.

The locked behavior is illustrated in Fig. 6. The DRL is locked to an RF frequency synthesizer. The tone is scanned and the control voltage and relative time of the signal through the delay path are recorded. The time delay variation is normalized to a single stage delay. Fig. 5 demonstrates close agreement with the predictions of an imperfect integrating loop and the measurements.

The delay path consumes 5mA at 3.3V per stage and has four stages to generate a 100ps delay. The DRL consumes 15mA at 3.3V. The current overhead introduced by the DRL is minimal in circuits that rely on a large number of time delay stages such as a transversal equalizer.

Two data eyes are presented in Fig. 7 to compare the performance at 5 and 10Gb/s.

V. Conclusion

This work proposes the active analog delay as a realization for true time delay in equalizers and other broadband circuit applications. The active analog delay leverages smaller area and power requirements that scale with technology compared to transmission line and lumped LC lines. To implement the proposed active analog delay, a delay reference loop has been designed. The delay reference loop tracks the process, voltage, and temperature variations of the circuit with a stable reference frequency. A SiGe chip was fabricated that demonstrates the delay-reference loop operation at 5GB/s and 10GB/s. This work has

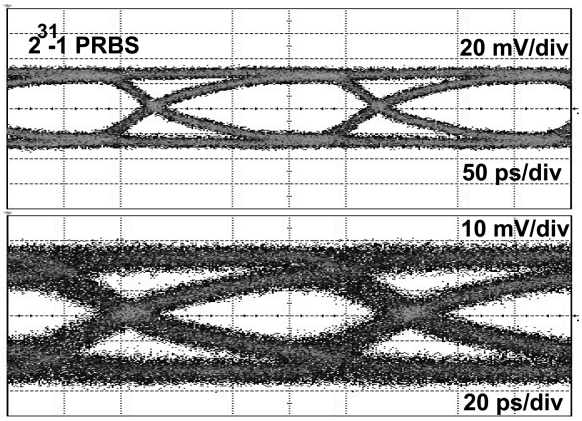

Fig. 7. Eye diagram at 5Gb/s and 10Gb/s for the active analog delay stage.

demonstrated a broadband analog delay stage that operates up to 10 Gb/s and occupies less than 10% of the area of comparable passive delays. A delay reference loop has been designed to maintain the proper delay over PVT variations.

Acknowledgment

We would like to thank Behnam Analui and Hossein Hashemi for their guidance and the members of CHIC at Caltech for suggestions about the design, and IBM corp. for chip fabrication.

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