A Wideband 77GHz, 17.5dBm Power Amplifier in Silicon

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Abstract

A 77GHz, +17.5dBm fully-integrated power amplifier (PA) with 50Ω input and output matching is fabricated in a 0.12μm SiGe BiCMOS process. The power amplifier achieves a peak power gain of 17dB and a maximum single-ended output power of +17.5dBm with 12.8% of power-added efficiency (PAE). It has a 3dB bandwidth of 15GHz and draws 165mA from a 1.8V supply. Microstrip tubs are used as the transmission line structure resulting in large isolation between adjacent lines, enabling integration of the PA in a small area of 0.6mm^2.

I. Introduction

Higher frequency millimeter (mm) wave bands offer exciting opportunities for various applications such as short-range communication (*e.g.*, 60GHz band) and automotive radar (*e.g.*, 77GHz band) [1][2][3]. Penetration of silicon integrated circuits into these bands can bring the unchallenged reign of compound semiconductors at these frequencies to an end. The unmatched levels of integration offered by silicon integrated circuits will enable a new level of integration and novel architectures encompassing microwave, analog, and digital blocks [4][5].

Perhaps the most challenging building block at mm-wave frequencies is the power amplifier (PA). The continued scaling of the transistor dimensions results in an inevitable reduction in the breakdown voltages that in turn aggravates the PA design challenges and necessitates novel design techniques at high frequencies. On the other hand, the mm-wave frequencies facilitate the use of on-chip transmission lines for power combing and impedance matching while providing high levels of on-chip isolation between various blocks. Such liberal use of transmission lines at lower frequencies is prohibited by their length (and hence loss). These concepts are demonstrated in this paper through the design of a fully integrated 77GHz power amplifier in silicon.

II. Frequency Band

In a collision-avoidance automotive radar, in order to resolve cars that are closely spaced at a far away distance, a large antenna directivity is required. For example two cars in adjacent lanes (~ 3 meters apart) that are 100 meters away, have an angular separation of just 1.7^o. In a typical short and long-range vehicular radar a directivity of > 20dB and > 36dB is required, respectively [6]. With a typical ~8dB directivity of a patch antenna, approximately 9x4 and 33x31 array elements are needed for the short-range and long-range, respectively. This explains the need to operate at very high frequencies, such as 76-77GHz band, to be able to reduce the system size for such large number of elements.

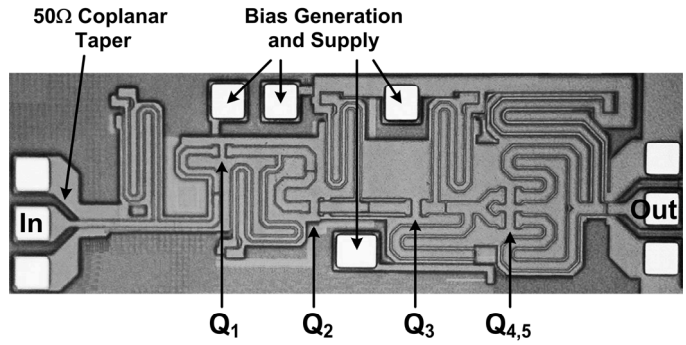

Fig. 1. Die micrograph of the 77GHz power amplifier, chip size: 1.35 x 0.45 mm^2.

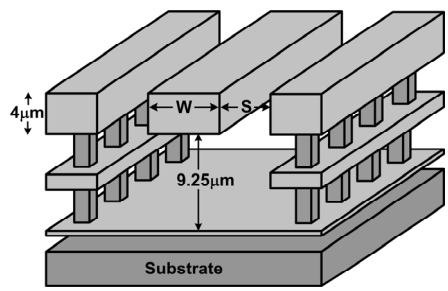

Fig. 2. Microstrip tub transmission line structure used for matching in the amplifier.

III. Amplifier Design

The power amplifier has been designed in a 0.12μm BiCMOS process featuring SiGe transistors with a cutoff frequency of $f_T \approx$ 200GHz [7]. Die photo of the amplifier is shown in Fig. 1. The back-end consists of 5 metal layers with three copper layers and a thick 4μm aluminum layer as top metal for low-loss interconnects. The breakdown voltages of the transistors are $BV_{CEO} \approx$ 1.7V and $BV_{CBO} \approx$ 5.5V. Substrate resistivity is ~ 14 Ω.cm.

A. Microstrip Tub as the Transmission Line Structure

The microstrip tub structure shown in Fig. 2 is used throughout the amplifier for matching. The presence of the side shields increases isolation between adjacent lines, allowing a compact layout. Fig. 3 shows the isolation between two adjacent 50Ω lines vs. their center-to-center spacing. The lines are

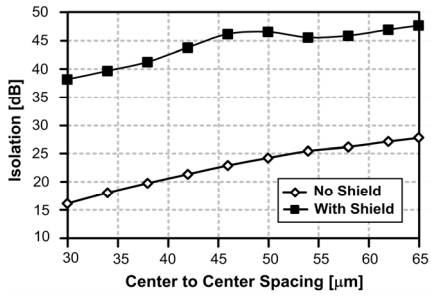

Fig. 3. The simulated isolation between two side-by-side 400μm, 50Ω microstrip lines with shield (W = 5μm, S = 7.5μm) and without shield (W = 13μm).

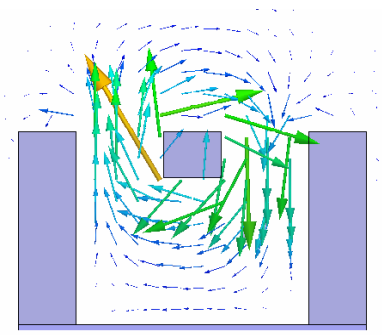

Fig. 4. The magnetic field distribution of the microstrip tub structure, showing most of the return current coming from the side shields.

implemented using the top three metals of the process. The lower two metals are left for routing of low frequency signals. The use of side shield increases isolation by more than 20dB. The transmission lines used in the amplifier are simulated using IE3D and their loss at 77GHz is less than 1.5dB/mm.

Fig. 4. shows the magnetic field distribution in the transmission line, simulated with a 3D field solver (Ansoft HFSS). Each arrow indicates the direction and magnitude of the magnetic field at the base of the arrow. The tangential component of the magnetic fields is a clear indication of the surface current in metals. As can be seen from the figure, the bottom plate carries very little current (small tangential component of the magnetic field) while the shield carries most of the return current. In this respect the structure behavior is more similar to a coplanar structure, with bottom metal isolating it from substrate. The tub shape also reduces surface wave propagation, improving isolation between elements and hence simplifying single-chip system integration. Since the PA is the highest-power block in a transceiver, it is critical to minimize the interference generated by PA to sensitive elements in the transceiver (such as VCO).

B. Circuit Architecture

The schematic of the amplifier is shown in Fig. 5. The amplifier consists of 4 gain stages, where output stage is designed for maximum efficiency and the other stages are designed for maximum gain. The last three stages use 1, 2, and 4 identical transistor cells. This geometric increase in transistor size from stage to stage ensures that the output transistors will enter compression first as long as the preceding stages have at least 3dB of gain. Carefully designed CPW tapers absorb pad parasitics, providing a 50Ω impedance at the input and output microstrip ports of the PA. All the transistors have single emitter stripe, use minimum emitter width of 0.12μm, and have two base

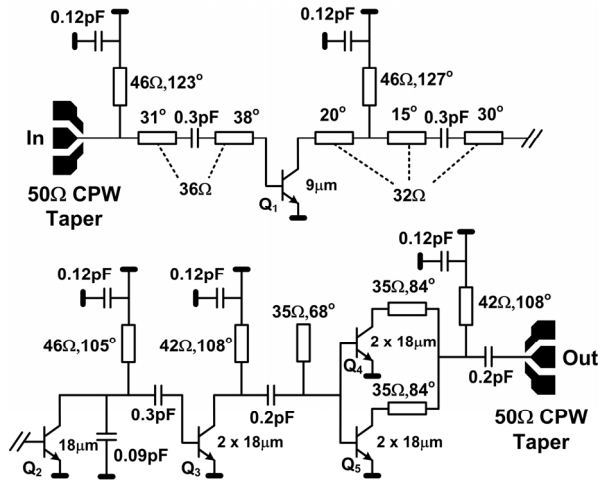

Fig. 5. Schematic of the 77GHz power amplifier including element values.

and collector contacts (CBEBC configuration). For reliable operation, the collector junction has more than the minimum number of contacts possible (three rows of long rectangular vias in parallel). The amplifier is biased in class-AB mode. Transistors are biased at their maximum f_{max} (1.2mA for 1μm of emitter length).

When the power amplifier is driven into saturation, the collector voltage of output transistor can go up to more than twice the supply voltage. A low open-base collector-emitter breakdown voltage, BV_{CEO}, of 1.7V limits the possible supply voltage to about 0.9V for a large drive impedance in the base.

In a normal silicon transistor, maximum dielectric breakdown field and velocity saturation pose a rather fundamental breakdown voltage vs. speed limitation [8][9]. But in the process used the BV_{CEO} limit is set by the impact ionization effect, in which the electron-hole pairs generated by accelerated electrons constitute base current. If the base is driven with lower source impedance this breakdown voltage will increase. In this case, voltage swing is limited by BV_{CER} rather than BV_{CEO}, where in the process used BV_{CER} is around 4V for R_B equal to 300Ω [3]. Therefore, the bias circuitry is designed to provide a base resistance of 300Ω for the transistors in the amplifier.

C. Design of the Matching Networks

The matching networks use series transmission lines and parallel shorted-stubs for power match between different stages. At input of the last stage an open stub provides lower matching network loss. At the output of second stage this was achieved with a parallel MIM capacitor.

The capacitors at the end of shorted parallel stubs are in parallel with a series RC network (which is not shown in Fig. 5 for simplicity). Careful choice of R and C reduces gain of the amplifier at low frequencies, enhancing stability.

The optimum impedance at the collector of each stage is determined with a large-signal power match. Similar to [10], a load pull simulation is performed to find the best load for the transistor. For the output stage this point is chosen to maximize the efficiency and for the other stages to maximize gain. Fig. 6 shows the result of the load pull simulations for all the four

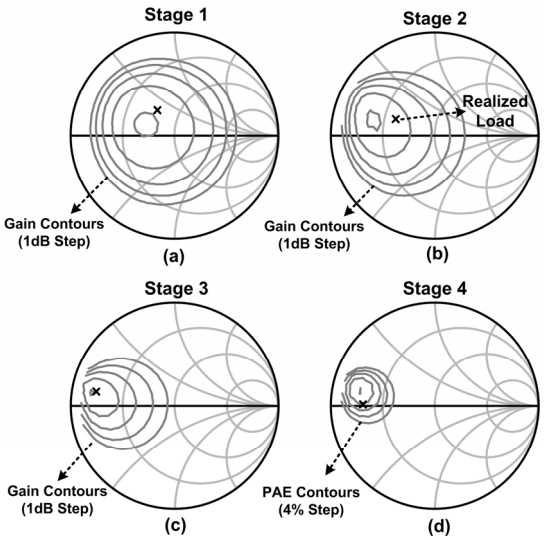

Fig. 6. Load pull simulation of the four stages of the power amplifier, together with the actual realized load impedances.

stages. These gain and PAE contours have steps of 1dB and 4%, respectively. The contours become denser as we move toward the output stage, indicating larger sensitivity of the amplifier to matching errors.

The realized impedance is not exactly at the center of the contours. This is more obvious in the case of output stage where the realized load provides a PAE that is 4% lower than maximum possible PAE. This is because the optimum load impedance is not the only criterion in the design of the matching network. Loss of the matching network also needs to be minimized during the design of matching network. A weighted least-mean-square optimization with gradient-descent scheme was used to choose the length and characteristic impedance of the matching networks. The optimization goal is to minimize the sum of the squares of the distance to the optimum load point and the loss in the matching network simultaneously. Therefore, for having a reasonable passive efficiency, the realized load is not exactly at the center of load pull contours. Due to a higher sensitivity of the output stage to mismatch, a slightly different design criterion was chosen for the output stage. Consequently, the output stage has the largest passive loss (2.2dB).

D. *Simulation and Layout Methodology*

The circuit was simulated in ADS. Electromagnetic simulations based on method of moments were performed using IE3D to design coplanar tapers and verify transmission line models and non-idealities like bends and T-junctions.

Parasitic capacitors are extracted on local nodes where the capacitance is not part of the distributed transmission-line structure. These nodes include connections to transistors, where top-level signal should travel to the lower levels closer to substrate. Parasitic collector-base capacitance is very important as it will be multiplied due to the Miller effect and appear at input or can even cause oscillation. Careful layout techniques minimized the overlap of the collector and base connections and reduced this parasitic capacitor to less than 1fF for all the transistors.

E. *Wideband Design*

Although the parasitic layout capacitances can be absorbed into the matching networks, they reduce bandwidth of the amplifier. One way to explain this behavior is by the Bode-Fano criterion [11]. If a lossless network is used to match a parallel RC load, there is an upper limit on the broadband match that can be achieved. More specifically:

$$\int_0^{\infty} ln \frac{1}{|\Gamma(\omega)|} d\omega \le \frac{\pi}{RC}$$

where $\Gamma(\omega)$ is the reflection coefficient seen looking into the arbitrary lossless matching network. Therefore by increasing the load capacitance the quality of the match will degrade, *i.e.*, either the reflection coefficient must increase or the bandwidth has to be reduced. Though it's possible to have a wideband and flat gain by introducing large mismatch [11], load pull simulations in Fig. 6 show that the resulting mismatch will decrease gain and PAE of the amplifier, significantly, particularly at the output stage.

We minimized parasitic capacitances by a vertical wedge-type via array. The largest ratio of parasitic capacitance to device capacitance (60%) occurs at the output of the first stage, with 16.5fF parasitic capacitance.

IV. Measurement Setup

The small-signal gain of the amplifier was measured with HP 8757E scalar network analyzer. The network analyzer sweeps the output frequency of a high-power W-band back-wave oscillator (BWO) from Resonance Instruments Inc. This is done with a 705B millimeter wave sweeper from Micro-Now Instrument Co. The signal is fed through a WR-10 waveguide to a Pico-Probe WR-10 GSG probe. To calibrate the network analyzer first a thru measurement was done and then the PA was inserted in place of the thru.

The BWO has a fixed output power, which changes with frequency. To measure large-signal parameters of the amplifier, a variable attenuator (Millitech DRA-10-R000) with Agilent W8486A W-band power sensor was used. The loss of the probe was measured and de-embedded.

V. Measurement Results

The simulated and measured small-signal gain of the amplifier is shown in Fig. 7. The amplifier has a peak gain of 17dB around 75GHz. Normally the W-band waveguide measurement setup is used for 75-110GHz band, but the TE10 mode cutoff frequency for this waveguide is 59GHz and will not affect the measurement results between 65-75GHz significantly. The amplifier has a 3dB bandwidth of at least 15GHz and has gain up to 94GHz. A good match between simulated and measured results is observed.

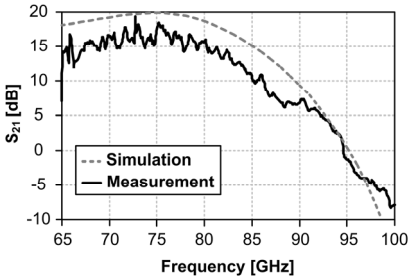

Fig. 7. Small-signal gain (S_{21}) of the amplifier simulated and measured between 65GHz and 100GHz.

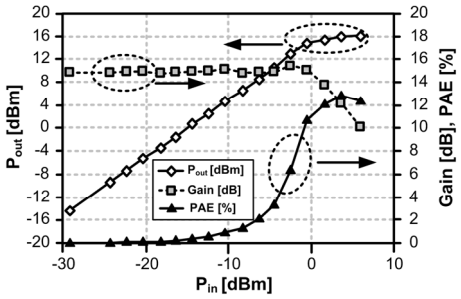

Fig. 8. Measured large-signal parameters of the amplifier at 77GHz.

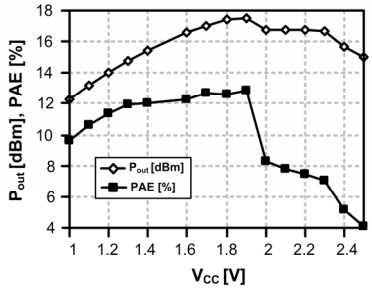

Fig. 9. Measured saturated power and PAE for a supply range of 1-2.5V.

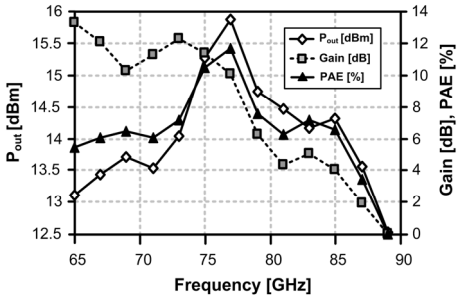

Fig. 10. Measured saturated power, gain and PAE vs. frequency.

The large-signal parameters of the amplifier are measured and plotted in Fig. 8. This is measured with a supply voltage of 1.5V. Amplifier can generate up to +16dBm, with a compressed gain of 10dB. A peak PAE of 12.8% is achieved at peak output power. The output-referred 1dB compression point of the amplifier is 14.5dBm. Additional gain and power in the input stages forces the output stage to compress first.

The variation of output saturated power and PAE vs. supply voltage is measured and shown in Fig. 9. Here the amplifier is driven with a constant +6dBm input power. Peak output power of 17.5dBm can be generated with a supply voltage of 1.8V.

The measured saturated power, gain and PAE of the amplifier vs. frequency are shown in Fig. 10. Peak power and maximum PAE happen exactly at 77GHz, showing the effectiveness of the large-signal power match design methodology outlined in section III.C.

VI. Conclusion

Microstrip tub structure with large isolation has been used to make a 77GHz power amplifier, fully-integrated in a 0.12µm BiCMOS SiGe process. Amplifier has more than 6dB small-signal gain in a frequency range of 65-95GHz. The measurement of the gain at frequencies lower than 65GHz is limited by frequency range of the measurement equipment. Large-signal power match has resulted in peak power and PAE occurring at 77GHz. The amplifier operates reliably above the BV_{CEO} range by proper choice of impedance in base and can be used with a supply range of 1V to 2.5V. A comparison of the power amplifier is this work and previous work on mm-wave power amplifiers (mostly in silicon) is summarized in Table I.

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Table I. Comparison

Freq.	Device	P_{out} [dBm]	PAE_{max} [%]	Gain [dB]	Ref.
77GHz	0.12µm SiGe	17.5	12.8	17	This Work
77GHz	0.12µm SiGe	10	3.5	6.1	[2]
60GHz	0.12µm SiGe	16	4.3	10.8	[3]
90GHz	0.1µm GaAs pHEMPT	21	8	19	[9]

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