Brief Papers

A 24-GHz CMOS Front-End

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***Abstract*—This paper reports the first 24-GHz CMOS front-end in a 0.18-μm process. It consists of a low-noise amplifier (LNA) and a mixer and downconverts an RF input at 24 GHz to an IF of 5 GHz. It has a power gain of 27.5 dB and an overall noise figure of 7.7 dB with an input return loss, S_{11} of -21 dB consuming 20 mA from a 1.5-V supply. The LNA achieves a power gain of 15 dB and a noise figure of 6 dB on 16 mA of dc current. The LNA's input stage utilizes a common-gate with resistive feedthrough topology. The performance analysis of this topology predicts the experimental results with good accuracy.**

***Index Terms*—CMOS analog integrated circuits, integrated circuits noise, receiver front-ends, RF amplifiers, wireless communications.**

I. Introduction

THE rapid evolution of wireless communications has resulted in a strong drive toward building high-performance RF circuits in silicon, particularly CMOS, for its low cost and high level of integration. Meanwhile, the growing demand for larger bandwidth motivates integrated circuits to move toward higher frequencies. Recent works have shown CMOS as a promising medium for building RF circuits in the low-gigahertz range [1]–[4]. However, a high-performance CMOS front-end for applications above 20 GHz has not been reported to date. These high frequencies provide higher available bandwidth and make it possible to use small-sized phased array antennas [5] for beam forming [6], [7] and space-time coding [8]. The purpose of this work is to develop a CMOS receiver front-end (LNA+mixer) operating at frequencies above 20 GHz (i.e., 24-GHz industrial, scientific, and medical (ISM) band).

A simplified block diagram of a typical receiver is shown in Fig. 1. In this architecture, the RF amplification and downconversion stages are the most critical to the system noise performance and the most challenging to implement in CMOS. This work reports the design and implementation of a 24-GHz CMOS front-end. Section II presents a novel low-noise amplifier (LNA) topology, common-gate with resistive feedthrough. Section III describes the circuit design and implementation of the front-end in detail. The experimental results are shown and discussed in Section IV.

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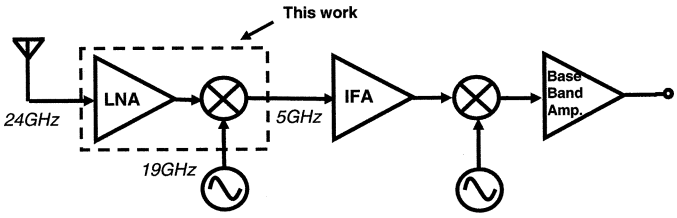

Fig. 1. 24-GHz receiver.

II. LNA Analysis

Lower intrinsic gain of transistors makes it more difficult to achieve low noise figure (NF) at very high frequencies. Additional noise sources, such as gate-induced noise, become more prominent with increasing frequency. Therefore, it is necessary to re-evaluate the topologies used for such LNAs.

A. Common-Source and Common-Gate LNAs

The common-source stage with inductive degeneration has been commonly used in CMOS LNA implementations [1]–[3], [10]–[15]. Extended analysis of this topology has been given in many previous publications [13], [14]. It can be shown that for an input-matched common-source LNA, the minimum achievable noise factor, $F_{\min}$, and the effective transconductance, G_m, are linearly related to the working frequency, ω_0 and $1/\omega_0$, respectively [13]. Therefore, although this common-source topology is well suited for applications at low-gigahertz range, its performance degrades substantially at higher frequencies when ω_0 becomes comparable to ω_T [9], [15].

In contrast, in the common-gate (CG) LNA, the gate-source and gate-drain parasitic capacitances of the transistor are absorbed into the *LC* tank and resonated out at operation frequency. Therefore, to the first order, the noise and gain performance of the common-gate stage are independent of the operation frequency, which is a desirable feature for high-frequency design. However, due to the constraints of input matching, it can be shown that the noise factor of the CG LNA has a lower bound of $1 + \gamma$ for perfect input match, where γ is the channel thermal noise coefficient. In the following subsection, a resistive feedthrough technique is proposed to bring the noise factor of common-gate LNA to a significantly lower level.

B. Common-Gate With Resistive Feedthrough LNA

Most analysis on CG LNA assumes the transistor output resistance r_{ds} is infinite. It was first noted in [16] that a finite r_{ds} of the input transistor increases input resistance and can be used

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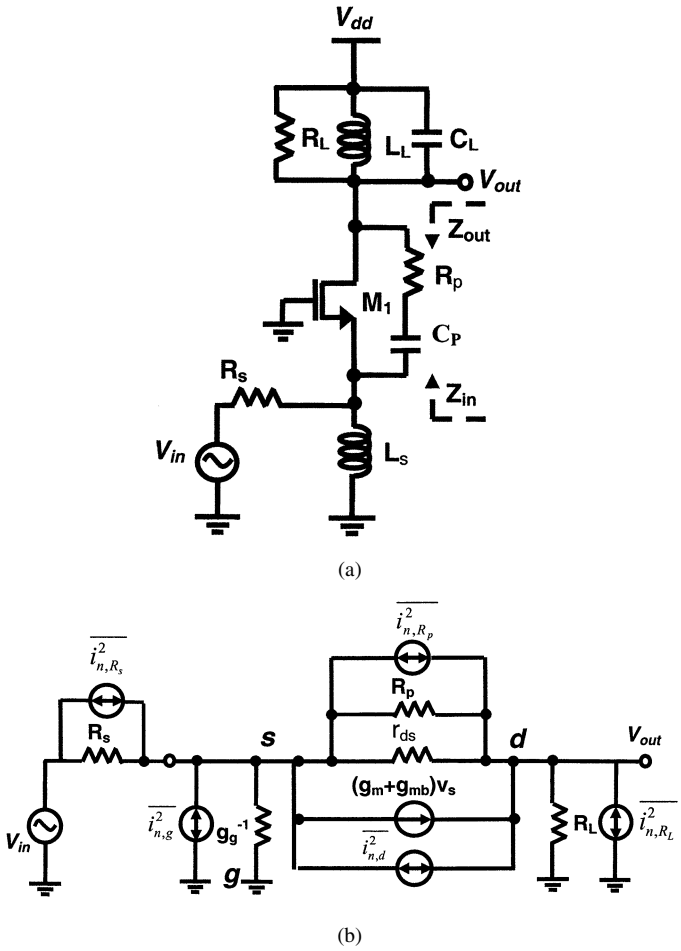

Fig. 2. Common-gate with resistive feedthrough LNA. (a) Schematic. (b) Small-signal equivalent circuits.

to build CG LNA with noise factor lower than the bound of $1+\gamma$. The transistor output resistance depends on the channel length and bias current, so the designer cannot control its value freely. We can add an external resistor, R_p, to the traditional CG LNA in parallel with the input transistor to improve its noise performance, as Fig. 2(a) shows. We call this topology common-gate with resistive feedthrough (CGRF) LNA. A detailed analysis of this stage is given next.

In Fig. 2(a), R_s is the signal source impedance, C_p is a large capacitor for isolating dc level, and R_L is the resistive load at the drain of M_1 owing to the finite quality factor Q of the resonant load. Inductors L_L and L_s resonate at operation frequency with capacitive load at drain and source of M_1, respectively.

The small-signal equivalent circuit of the CGRF LNA at operation frequency is shown in Fig. 2(b), including the major noise sources, where g_m is the transistor transconductance, g_{mb} is the backgate transconductance, g_g is the real part of the gate admittance [17], $\overline{i_{n,d}^2}$ is the transistor channel thermal noise source, and $\overline{i_{n,g}^2}$ is the induced gate noise source [17].

The analysis starts with the study of the circuits at low frequency, where $\overline{i_{n,g}^2}$ and g_g can be neglected. We will include the effect of these terms later. The feedthrough resistor R_f, which is formed by R_p in parallel with r_{ds}, creates a positive feedback loop around the amplifier to enhance the input impedance. Analysis of the circuit in Fig. 2(b) shows that at resonance frequency, the input impedance seen looking into the source of M_1 can be expressed as

$$Z_{\text{in}} = \frac{R_f + R_L}{1 + g_m R_f (1+\chi)} \tag{1}$$

where g_m is the transistor transconductance, χ is the ratio of the transistor backgate transconductance g_{mb} to g_m, and $R_f = R_p \| r_{ds}$.

If input is matched, the effective transconductance of CGRF stage is given by

$$G_{m,\text{CGRF}} = \frac{1}{2R_s} \tag{2}$$

which indicates that to the first order at input matching condition the gain of CGRF stage is independent of R_f and g_m.

Assuming a matched input and $R_s \ll R_L$, it can be shown that the output noise power generated by the thermal noise of R_p and R_L is negligible compared to that generated by the transistor channel thermal noise, and the noise factor can thus be approximately expressed as

$$F_{\text{CGRF}} \approx 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\chi}\right)^2 \frac{1}{g_m R_s} \tag{3}$$

where α is the ratio of g_m to the channel conductance at zero drain-to-source voltage g_{d0}. Based on the simplifying assumptions that ignore gate noise and g_g, it may appear that the noise of CGRF amplifier can approach 0 dB by increasing g_m, providing a direct way to trade between power and noise while keeping the input matched [9].

However, at high frequencies, we should include the effect that the coupling between channel and gate is due to a distributed *RC* network, reflected in the real part of the gate admittance, g_g. In the pinch-off region, g_g is related to operation frequency ω_0, gate-source capacitor C_{gs}, and g_{d0} through [13], [17]

$$g_g = \frac{C_{\text{gs}}^2 \omega_0^2}{5 g_{d0}}. \tag{4}$$

This conductance has a thermal noise $\overline{i_{n,g}^2}$ associated with it, which is called induced gate noise. The power spectral density of $\overline{i_{n,g}^2}$ is given by [17]

$$\frac{\overline{i_{n,g}^2}}{\Delta f} = 4kT\delta g_g \tag{5}$$

where δ is the gate noise coefficient. $\overline{i_{n,d}^2}$ and $\overline{i_{n,g}^2}$ are partially correlated with a complex correlation coefficient c given by

$$c = \frac{\overline{i_{n,g} i_{n,d}^*}}{\sqrt{\overline{i_{n,g}^2}\,\overline{i_{n,d}^2}}}. \tag{6}$$

Taking g_g into account, the input impedance of CGRF stage is revised as

$$Z_{\text{in}} = \left(\frac{1 + g_m R_f (1+\chi)}{R_f + R_L} + \eta(\omega_0) g_m\right)^{-1} \tag{7}$$

where $\eta(\omega_0)$ is defined as the ratio between g_g and g_m, i.e.,

$$\eta(\omega_0) \equiv \frac{g_g}{g_m} \approx \frac{\alpha}{5}\left(\frac{\omega_0}{\omega_T}\right)^2. \tag{8}$$

If input is perfectly matched to R_S, the effective transconductance of the CGRF stage is given by

$$G_{m,\mathrm{CGRF}} = \frac{1}{2R_s}[1 - g_m R_s \eta(\omega_0)] \tag{9}$$

which indicates that a large g_m or high frequency can degrade the gain. This is because an increase of g_m or frequency results in a larger g_g, making more signal loss through the gate.

Assuming a matched input and $R_s \ll R_L$ yields the following expression for F:

$$\begin{aligned} F_{\mathrm{CGRF}} \approx & 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\chi}\right)^2 \\ & \times \left(\frac{1}{g_m R_s} + \eta^2(\omega_0) g_m R_s + 2\eta(\omega_0)\right) \\ & + \delta\eta(\omega_0) g_m R_S \end{aligned} \tag{10}$$

where the second term represents the contribution of channel thermal noise and the third term represents the contribution of induced gate noise. At low frequencies, $\eta(\omega_0) \rightarrow 0$, (10) reduces to (3).

It can be shown that an optimum g_m exists for minimum noise figure, i.e.,

$$g_{m,\mathrm{CGRF,opt}} = \frac{1}{R_s}\left(\frac{\delta\alpha}{\gamma}(1+\chi)^2\eta(\omega_0) + \eta^2(\omega_0)\right)^{-\frac{1}{2}}. \tag{11}$$

The corresponding minimum F is approximately given by

$$F_{\mathrm{CGRF,min}} \approx 1 + \frac{\gamma}{1+\chi}\left(\sqrt{\frac{4\delta}{5\gamma}}\left(\frac{\omega_0}{\omega_T}\right) + \frac{2}{5(1+\chi)}\left(\frac{\omega_0}{\omega_T}\right)^2\right). \tag{12}$$

C. Stability

Since in the CGRF stage, R_f results in positive feedback, the stability issue needs to be carefully addressed. Considering the input transistor with feedthrough resistor in Fig. 2(a) as a two-port network, Z_S and Z_L are the load impedance at the two ports, source and drain, respectively. It is a sufficient condition to prevent oscillation that the real part of both impedance seen looking into the ports Z_{in} and Z_{out} are positive. It is easy to shown that $\mathrm{Re}[Z_{\mathrm{in}}]$ and $\mathrm{Re}[Z_{\mathrm{out}}]$ can be expressed as

$$\mathrm{Re}[Z_{\mathrm{in}}] = \frac{R_f + \mathrm{Re}[Z_L]}{1 + g_m R_f(1+\chi)} \tag{13}$$

$$\mathrm{Re}[Z_{\mathrm{out}}] = R_f + [g_m R_f(1+\chi) + 1]\mathrm{Re}[Z_S] \tag{14}$$

where $R_f = R_p \| r_{ds}$, and (13) and (14) indicate that as long as $\mathrm{Re}[Z_L]$ and $\mathrm{Re}[Z_S]$ are positive, the stability of the CGRF stage is guaranteed.

III. Circuit Design and Layout Issues

A. 24-GHz LNA

The analysis in the previous section ignores all the substrate effects. However, at 24 GHz, capacitive coupling and resistive loss through substrate have considerable influence on the circuit performance. A simplified substrate network model for MOS transistor is shown in Fig. 3 [18]. Simulation results show the capacitive coupling between drain and source through this network harms stability and noise figure. A shunt inductor L_p in series with a large bypass capacitor C_p can be added, as shown in Fig. 3, to resonate the equivalent capacitance between drain and source so that the substrate effects are reduced. The series resistance of L_p can be converted to an equivalent parallel resistance, which affects the performance of the LNA as a feedthrough resistor. In this case, the feedthrough resistance can be expressed as

$$R_f = Q\omega_0 L_p \| r_{ds} \tag{15}$$

where Q is the quality factor of L_p.

Fig. 4(a) shows the 24-GHz CMOS LNA. It consists of three stages. The first stage employs CGRF topology, where shunt inductor L_2 resonates the capacitive coupling while introduces a feedthrough resistance given by (15) between drain and source

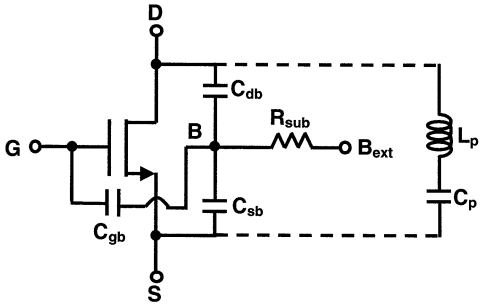

Fig. 3. Reducing substrate coupling by using parallel inductor.

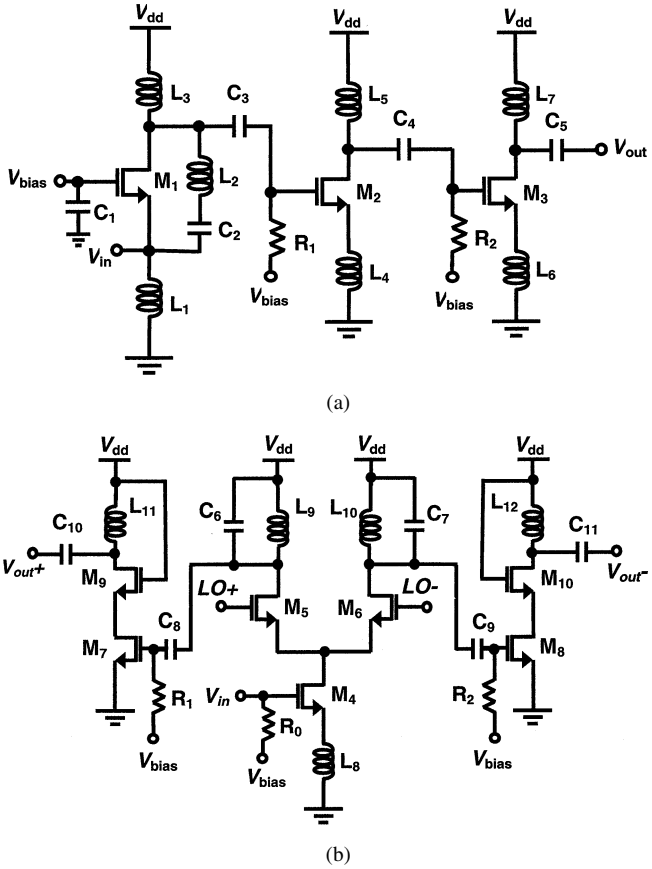

Fig. 4. Building blocks. (a) Three-stage LNA. (b) Downconversion mixer.

of M_1. A 1-pF MIM capacitor C_2 isolates the dc level of source and drain. The second and third stages are both common-source with inductive degeneration amplifiers which are used to enhance the overall gain.

The peak f_T of the 0.18-μm CMOS device used at 1.5 V bias is about 60 GHz. To achieve the minimum noise figure at 24 GHz, the optimum g_{m1} is estimated to be about 80 mS by using (11). To reduce the power consumption, we choose g_{m1} to be 40 mS in this design. We also lower $(V_{\rm gs}-V_t)$ by a factor of two from its value for peak f_T, which is a more power-efficient way reducing current consumption by more than 50%, while reducing f_T by only about 10%. Finally, M_1 is biased at 8 mA with 54-GHz f_T. The second and third stages consume 4 mA each.

Since the feedthrough resistor is replaced by an inductor in the first stage in Fig. 4(a), the stability of the amplifier needs to be reexamined. Simulation shows that the first stage is unconditionally stable up to 43 GHz. Above 43 GHz, the stability factor of the stage K_f is less than one. However, the input impedance of the second stage is located in the stable region with sufficient margin. Stable operation in all frequency ranges is observed in both simulation and measurement.

B. 24-GHz to 5-GHz Mixer

The core of the mixer shown in Fig. 4(b) is a conventional single-balanced Gilbert-type mixer. The RF input applies at the gate of M_4 which is used as a transconductance amplifier. The linearity of this transconductance amplifier is improved by using source degeneration inductor L_8, which also adjusts the input impedance seen looking into the gate of M_4 in order to improve the impedance matching at the LNA-mixer interface. The M_4 is biased at 4-mA dc current.

The chopping function is accomplished by the $M_5 \sim M_6$ mixing cell, and 1.6-V peak-to-peak differential local oscillator (LO) signal is applied. Cascode amplifiers following the differential mixing cell are used to drive the 50-Ω loads. The output-match is accomplished by the *LC* impedance transforming network.

C. Layout Issues

The circuit has been designed and fabricated using 0.18-μm CMOS transistors. The process offers six metal layers with two top layers of 1-μm-thick copper. L_4 and L_6 in the LNA and L_8 in the mixer are slab inductors, and all the other inductors are spirals.

Shielded pads [19] are employed at both RF and IF ports. Grounded metal1 underneath the pads prevents loss of the signal power and noise generation associated with the substrate resistance. Ground rings are placed around each transistor at minimum distance to reduce the substrate loss. Separated $V_{\rm dd}$ pads are assigned to the LNA, mixer, and bias circuits. Large on-chip bypass capacitors are placed between each $V_{\rm dd}$ and ground.

The die micrograph is shown in Fig. 5. The size of the chip is 0.8×0.9 mm^2 including a large area occupied by the wide ground rings and pads. The size of the core cell is only 0.4×0.5 mm^2.

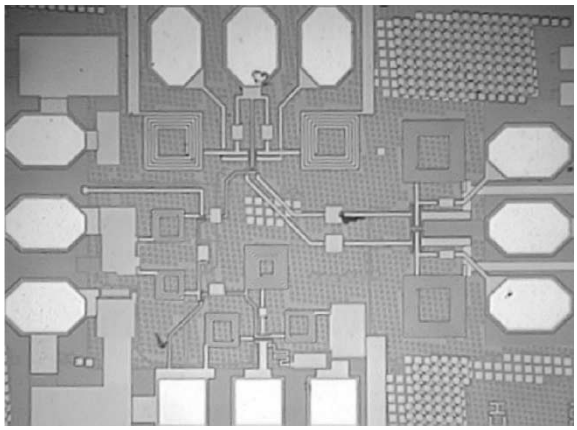

Fig. 5. Die micrograph.

TABLE I
PERFORMANCE SUMMARY OF THE 24-GHz FRONT-END

Parameters	Overall Front-end	LNA	Mixer
S_{11}	-21 dB	-21 dB	--
S_{22}	-10 dB	--	-10 dB
Peak Frequency	21.8 GHz RF	21.8 GHz RF	4.9 GHz IF
Power Gain	27.5 dB	15 dB	13 dB
Voltage Gain	35.7 dB	--	--
Noise Figure	7.7 dB	6 dB	17.5 dB
1-dB Compression Point	-23 dBm	--	--
Image Rejection	31 dB	--	--
Current Consumption	43 mA	16 mA	4 mA core cell + 23 mA output buffers
Supply Voltage	1.5 V	1.5 V	1.5 V
Chip Area	0.4 x 0.5mm^2	0.2 x 0.25 mm^2	--

IV. EXPERIMENTAL RESULTS

The front-end is tested by probing the input, output, and LO ports. The power and ground pads are wirebonded to the testing board. The reflection coefficients at the RF and IF ports are measured using an HP 8722D network analyzer. Conversion gain and noise figure are measured using an HP 8970B noise figure meter with an HP 8971 noise figure test set as a second downconverter. Table I summarizes the measured results of the front-end and the de-embedded performance of the LNA and the mixer. Fig. 6(a) shows the measured input and output reflection coefficients, S_{11} and S_{22}. The RF input and the IF output are well matched at their respective frequencies. Fig. 6(b) shows the measured power gain and extracted voltage gain with a 16.9-GHz LO frequency. The measurement shows that a 27.5 dB maximum power gain appears for an RF of 21.8 GHz and an IF of 4.9 GHz. The frequency offset from the 24 GHz is likely due to inaccurate modeling of MOS transistor and planar inductor at high frequencies. The LNA achieves a 15-dB power gain. The mixer followed further enhances the signal power by 13 dB. Because of the imperfect conjugate matching at the LNA–mixer interface, the overall power gain

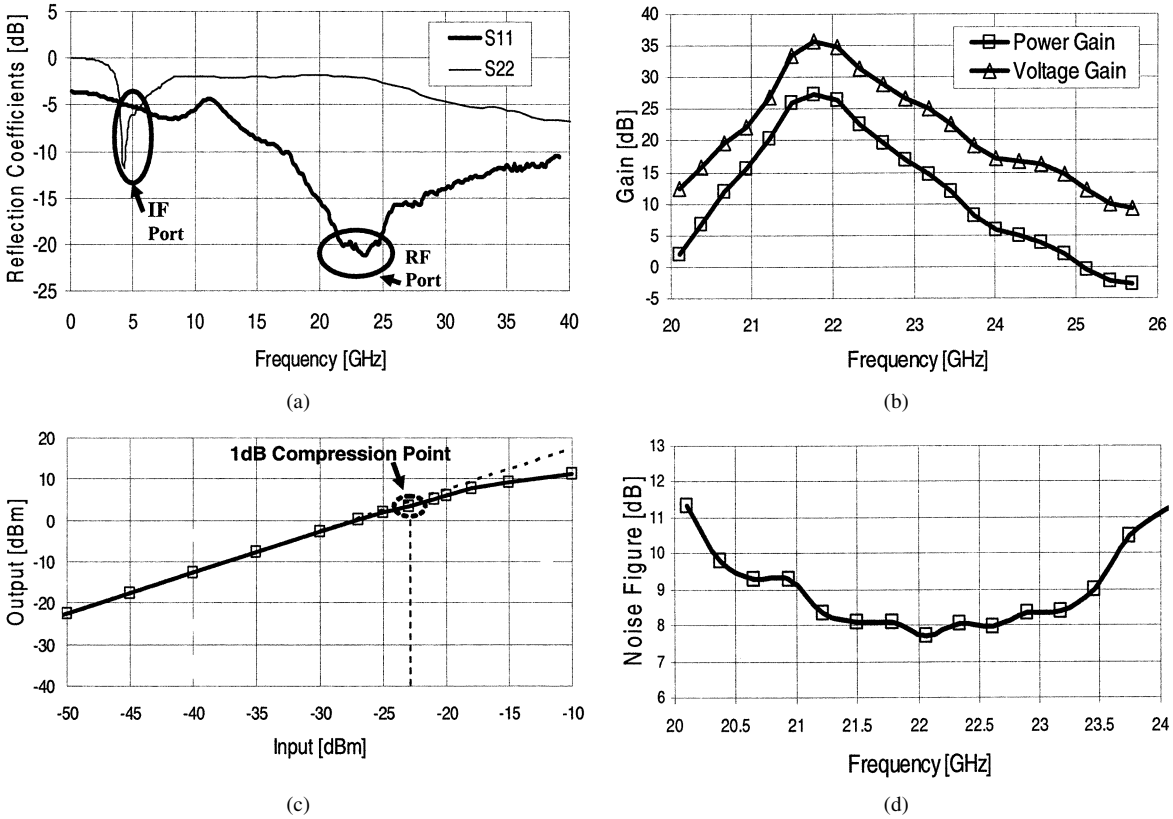

Fig. 6. Front-end measurement results. (a) Reflection coefficients. (b) Power gain and voltage gain (LO $=$ 16.9 GHz). (c) Large-signal nonlinearity. (d) Total noise figure of three-stage LNA + mixer (LO $=$ 16.9 GHz).

TABLE II
COMPARISON

	Device	Substrate	Freq.	Topology	Power Gain	NF	DC current
LNA in [15]	0.18-μm CMOS	Bulk	14.4GHz	common-source	21dB	8dB	18.6 mA
LNA in [20]	0.1-μm CMOS	SOI	23.8 GHz	common-gate	7.6 dB	10 dB	53 mA
This work	0.18-μm CMOS	Bulk	22 GHz	CGRF	15 dB	6 dB	16 mA

of the front-end is slightly lower than the sum of the individual power gain of the two blocks.

Fig. 6(c) and (d) reports the measured large-signal nonlinearity and noise figure, respectively. The input-referred 1-dB compression point of the front-end appears at -23 dBm. A minimum noise figure of 7.7 dB is achieved for the combined LNA and mixer at 22.08 GHz. The individual noise figures of the LNA and the mixer are 6 dB and 17.5 dB, respectively. The noise figure of the first CGRF stage is extracted to be 4.8 dB. Equation (3) predicts the $\overline{i_{n,d}^2}$ only noise figure of the first stage to be 3.3 dB. Equation (10) revises the prediction of the noise figure to be 4.1 dB by taking g_g and $\overline{i_{n,g}^2}$ into account; the remaining 0.7 dB is due to the thermal noise of the parasitic resistance and substrate noise.

The image rejection of the front-end is -31 dB. This performance is achieved via the large IF and the multistage nature of the LNA. The overall current consumption of the front-end is 43 mA, of which the output buffers consume 23 mA. The LNA and the mixer draw 16 and 4 mA, respectively, from a 1.5-V supply voltage. A comparison of the LNA in this work and the one in [15] and [20] is given in Table II.

V. CONCLUSION

The design issues and experimental results of a 24-GHz CMOS front-end are presented. A novel LNA topology, common-gate with resistive feedthrough, is studied and demonstrated with good performance at very high frequencies. The theoretical analysis of the LNA topology explains the experimental results. This work shows that CMOS technology is a viable candidate for building fully integrated receivers at frequencies higher than 20 GHz.

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