11.7 A 24GHz Phased-Array Transmitter in 0.18μm CMOS

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Integrated phased-array systems at high frequencies promise a future of low-cost radar and gigabit-per-second wireless communication networks. The improvements in the signal-to-noise-plus-interference ratio provided by phased-arrays and the larger bandwidths available at high frequencies motivate the implementation of phased-arrays at 24GHz [1,2]. A fully integrated 8-element 24GHz phased-array receiver has been already demonstrated [2]. In this paper, an integrated 24GHz 4-element phased-array transmitter in 0.18μm is presented that is capable of supporting data rates of more than 500Mb/s (limited by measurement setup). The fully integrated transmitter includes on-chip power amplifiers (PAs), with integrated 50Ω output matching.

Each element in a phased-array transmitter radiates the same signal delayed by different time intervals. As shown in Fig. 11.7.1, the transmitted outputs add up coherently in the desired direction, increasing the signal power. Incoherent addition of the outputs in other directions attenuates the signal power resulting in reduced interference at receivers that are not targeted. Electrical variation of the delay in each element permits steering of the main transmitter beam.

The architecture and the floorplan of the 4-element CMOS transmitter are shown in Fig. 11.7.2. The 24GHz transmitter is based on a two-step up-conversion architecture with an IF frequency of 4.8GHz. The delay required in each element is approximated by a phase shift in the LO path. As the mixers and the LO-path buffers operate in saturation, the variation of signal amplitude with LO-path phase shifting is minimal. Double-quadrature architecture is chosen for the up-conversion stages to attenuate the signal at image frequencies. The baseband input signals (I and Q) drive a pair of double-balanced Gilbert-type mixers in quadrature. The first set of mixers up-convert the baseband signal to 4.8GHz. These mixers are followed by in-phase and quadrature signal buffers (IF-I and IF-Q). A symmetric H-tree structure distributes the outputs of the 4.8GHz buffers to the 4.8GHz-to-24GHz up-conversion mixers in each path. The outputs of the second up-conversion mixers are buffered and fed to the PA drivers. At 24GHz, a 1% deviation in the center frequency of a tuned passive load translates to a tuning that is off by 240MHz. The cascade of tuned stages in the signal path compounds the sensitivity of the transmitter to the frequency tuning of the passive loads. Digitally switchable capacitors at the outputs of some of the high frequency tuned stages enable the adjustment of the center frequencies of these stages (Fig. 11.7.3).

Since all the circuits in the signal path up to, and including, the PA driver are differential while the two-stage PA is single-ended, an on-chip balun is implemented for differential to single-ended conversion. The passive balun is realized with a single-turn transformer to reduce capacitive coupling to the substrate. Electromagnetic simulations show an insertion loss of 1.5dB for the balun when input and output parasitic inductances are tuned out.

The four on-chip PAs have output stages similar to the stand-alone PA in [3]. A simplified schematic of the two-stage PA used in this design is shown in Fig. 11.7.3. The use of cascode transistor pairs in each stage increases breakdown voltage and stability. The output of the single-ended PA is matched to 50Ω. The matching networks in both stages of the PA are designed using low-loss shielded-substrate coplanar waveguides with an effective dielectric constant that is nearly 4 times that of silicon dioxide [4]. Consequently, there is almost 50% reduction in matching network size resulting in lower loss. Series RC networks are included in the inter-stage matching of the PA to guarantee low-frequency stability.

A 16-phase 19.2GHz CMOS VCO consisting of eight differential amplifiers with tuned loads connected in a ring structure, similar to [2], generates 16 phases of the LO signal with steps of 22.5° for LO phase shifting. The same frequency synthesizer loop generates LO frequencies for both up-conversion stages (19.2GHz and 4.8GHz) from a 75MHz reference.

The phase selectors in each transmitter path have independent access to all the phases of the VCO. The phase selection is done in two stages, the first stage selecting the desired VCO differential phase pair and the next stage selecting the appropriate polarity. The phase selectors can also be used as phase interpolators by selecting more than one phase pair at a time, thereby generating phases with resolution finer than 22.5°. Symmetric floorplanning and an H-tree based distribution structure ensure symmetry of the LO signals at each transmitter path; any asymmetry in the LO signal increases the power in the transmit side-lobes, generating interference and clutter for communication and radar systems. The digital frequency calibration data and the beam-steering information are loaded onto the chip through a digital serial interface.

Figure 11.7.4 shows the measured output power against radiation angle with 2 elements and with all 4 elements activated. The measured patterns, when compared to theory, demonstrate the proper functioning of the phased-array transmitter. The peak-to-null ratio with 4 elements active is larger than 23dB. The fully saturated output power for each PA is 14dBm. The PA output power with driver output of 0dBm is 7dBm. A concern with placing multiple power amplifiers on the same die is the coupling between them. The worst-case isolation between different paths, including the bond wires and the traces on the test PCB, is found to be better than 28dB. The quadrature image rejection of the first up-conversion step is 24dB. The image signal of the second up-conversion stage is at 14.4GHz. The driver and the PA further attenuate this signal resulting in more than 43dB attenuation. The output power spectral density (PSD) of the transmitter for 100Mb/s and 500Mb/s QPSK signals at 24GHz is shown in Fig. 11.7.5. The measured performance of the transmitter is summarized in Fig. 11.7.6.

The transmitter is implemented using 0.18μm CMOS transistors and draws 788mA (including 4 on-chip PAs) from a 2.5V supply. The process has five metal layers, with a 4μm-thick top metal layer. Figure 11.7.7 shows the die micrograph of the chip. The die occupies an area of 6.8mm×2.1mm.

Acknowledgements:
The authors thank H. Hashemi and X. Guan for their assistance and support.

References:
[1] Federal Communications Commission, FCC 02-04, Section 15.515.15.521
[2] H. Hashemi et al., "A Fully-Integrated 24GHz 8-path Phased-Array Receiver in Silicon," *ISSCC Dig. Tech. Papers,* pp. 390-391, Feb., 2004.
[3] A. Komijani et al., "A 24GHz, 14.5dBm Fully-Integrated Power Amplifier in 0.18μm CMOS," *CICC*, pp. 561-564, Oct., 2004.
[4] T.S.D Cheung et al., "On-Chip Interconnect for mm-Wave Applications Using an All-Copper Technology and Wavelength Reduction," *ISSCC Dig. Tech. Papers,* pp. 396-397, Feb., 2004.

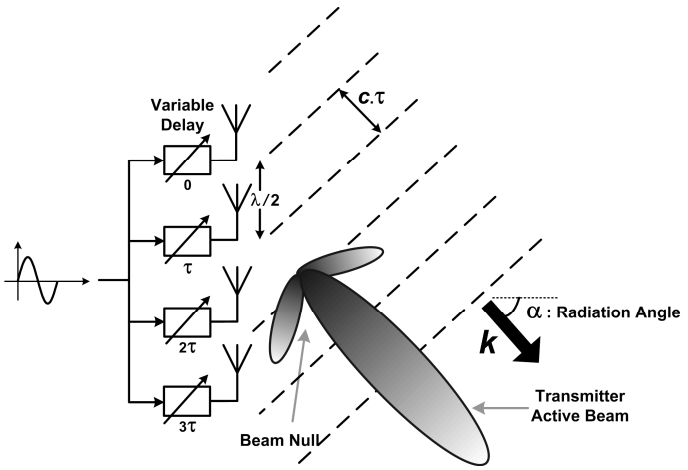

Figure 11.7.1: Beam forming in phased-array transmitter.

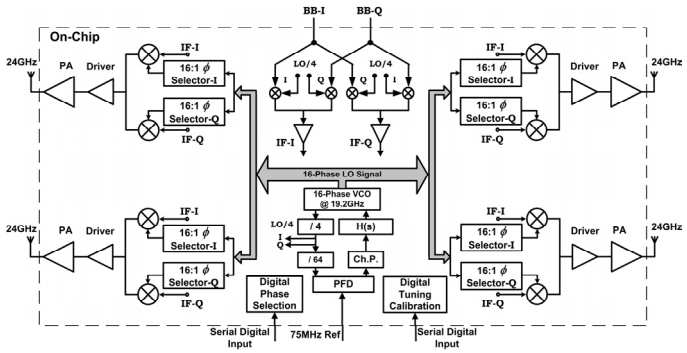

Figure 11.7.2: Architecture and floorplan of the proposed 4-element phased-array transmitter.

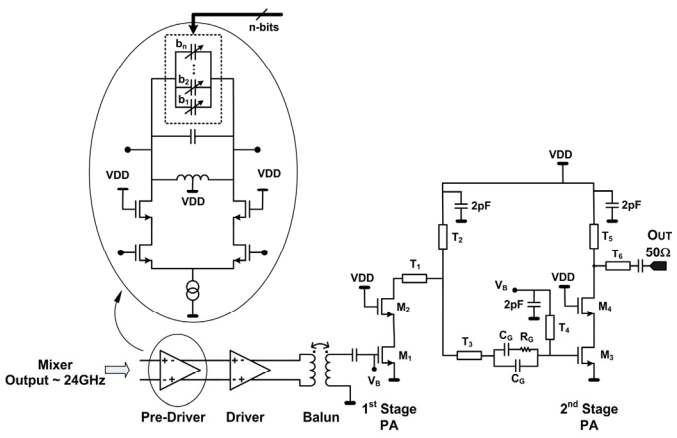

Figure 11.7.3: Schematic of PA driver and the PA.

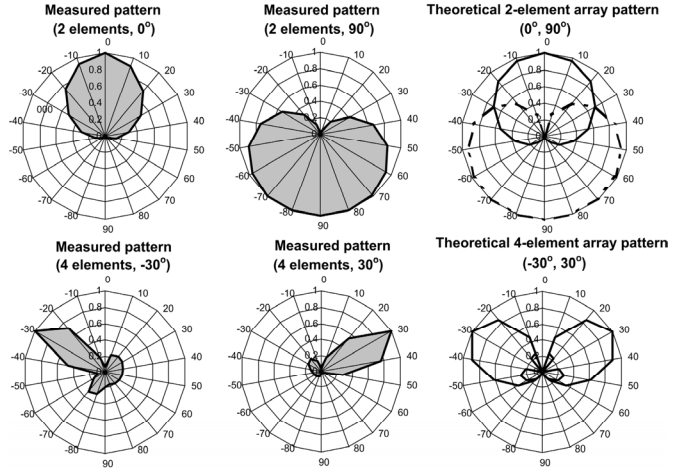

Figure 11.7.4: Theoretical and measured patterns for 2-element and 4-element arrays.

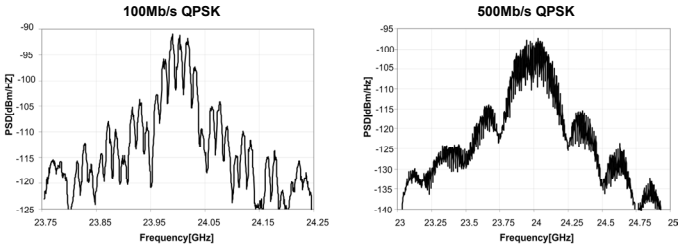

Figure 11.7.5: Measured output spectrum of 100Mb/s and 500Mb/s QPSK signals at 24GHz.

On-Chip CMOS Power Amplifier Performance	
Maximum Saturated Output Power	+14dBm
Current Consumption @ 2.5V	68mA
Output Match @ 24GHz	-20dB
Equivalent 4-element EIRP	+26dBm
Phased Array Performance	
Peak-to-Null Ratio for 4-element Array	> 23dB
Beam Steering Resolution	< 10° for normal radiation
3dB Array Beam-Width @ 30° Radiation Angle	17°
Isolation between Paths (including wire bonds)	> 28dB
Image Signal Attenuation	> 24dB, first up-conversion
	> 43dB, second up-conversion (image @ 14.4GHz)
Transmit 3dB Bandwidth	> 400MHz
Current Consumption @ 2.5V	
Signal Path (per element)	26mA
Phase Selector (per element)	34mA
16-Phase Frequency Synthesizer	180mA
Total (including IF stage and VCO buffers)	788mA
Device Technology	0.18μm CMOS
Die Area	6.8mm x 2.1mm

Figure 11.7.6: Summary of the transmitter performance.

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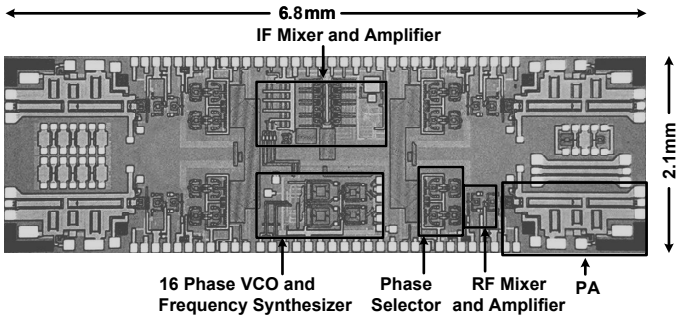

Figure 11.7.7: Die micrograph of the 24GHz CMOS phased-array transmitter.

