A 24-GHz SiGe Phased-Array Receiver—LO Phase-Shifting Approach

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***Abstract*—A local-oscillator phase-shifting approach is introduced to implement a fully integrated 24-GHz phased-array receiver using an SiGe technology. Sixteen phases of the local oscillator are generated in one oscillator core, resulting in a raw beam-forming accuracy of 4 bits. These phases are distributed to all eight receiving paths of the array by a symmetric network. The appropriate phase for each path is selected using high-frequency analog multiplexers. The raw beam-steering resolution of the array is better than 10° for a forward-looking angle, while the array spatial selectivity, without any amplitude correction, is better than 20 dB. The overall gain of the array is 61 dB, while the array improves the input signal-to-noise ratio by 9 dB.**

***Index Terms*—BiCMOS integrated circuits, phase-locked loops, phased arrays, radio receivers, silicon, voltage-controlled oscillators (VCOs).**

I. Introduction

PHASED ARRAYS are capable of beam forming and electronic steering by adjusting the relative phases of the signal received or transmitted by each antenna. In the past, the high price of discrete microwave modules limited the achievable complexity level of such systems for consumer applications. A low-cost fully integrated silicon-based phased-array transceiver facilitates widespread commercial applications such as ultrahigh-speed wireless communications and vehicular radar.

The Federal Communications Commission (FCC), has allocated 250 MHz of bandwidth around the 24-GHz frequency for unlicensed industrial, scientific, and medical (ISM) applications, in addition to field-disturbance sensors, as well as fixed and point-to-point wireless operation [1]. The FCC has also opened up a 7-GHz window between 22-29 GHz for ultrawideband vehicular radar systems [2]. Consequently, research on 24-GHz range wireless technologies has accelerated, demonstrating various building blocks and single path receivers at this frequency [4]–[7].

Compared to the 2.4- and 5-GHz frequencies that are commonly used for today's short-range wireless data communications schemes, the 24-GHz carrier frequency has a smaller associated wavelength that reduces the required size of the common resonant-based antennas and their spacing in a multiple antenna scheme. The smaller antenna size will, however, result in a reduced collected power at these higher frequencies. A recent study of an indoor wireless channel in an office environment at a variety of carrier frequencies [8] reveals that, at 24 GHz, the large absorbance of walls and ceilings results in more isolation between multiple floors and allows for increasing the frequency reuse and overall system capacity. It also shows that the 24-GHz carrier frequency can support a higher data rate due to lower delay spreads. The excess path loss at 24 GHz is more or less comparable to the 2.4- and 5.2-GHz bands due to the waveguide effect inside the building at higher frequencies.

To demonstrate the feasibility of a phased-array system on silicon and explore its advantages, we have implemented the first fully integrated 24-GHz phased-array receiver in silicon [3]. After a brief description of narrow-band phased arrays in Section II, we will focus on various architectural choices for a fully integrated phased-array receiver in Section III. The receiver architecture of an eight-path phased-array receiver based on a local-oscillator (LO) phase-shifting scheme will be presented in Section IV. Multiple LO phase generation and distribution are covered in Section V, followed by receiver array measured results in Section VI.

II. Narrow-Band Phased Arrays

When a plane electromagnetic (EM) wave arrives at an antenna array at an angle α with respect to the normal to array plane, the signal is received by each antenna at a different time due to the spatial path differences. In general, an angle-dependent time delay at the receiver can compensate the arrival delay and effectively focus the beam in a desired direction. In a one-dimensional array, the effective beam angle α is related to the delay difference of two adjacent elements ΔT, the spacing of two adjacent antennas D, and the speed of light c via

$$D \cdot \sin(\alpha) = c \cdot \Delta T. \tag{1}$$

With ideal delay elements following each antenna, the beam forming works independently of the frequency and bandwidth of the signal. Unfortunately, there are practical challenges to implementation of such broad-band tunable delay elements in the RF signal path, e.g., signal attenuation, noise, and linearity degradation, as well as signal dispersion. Fortunately, in many practical applications, such as wireless communications, the

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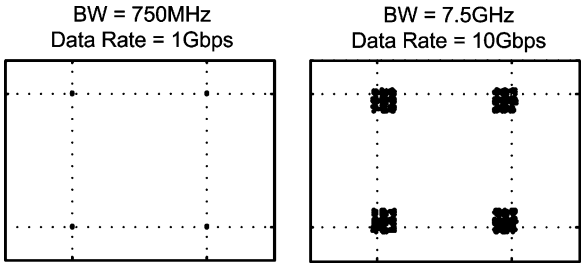

Fig. 1. Output signal constellation of an eight-path narrow-band phased-array receiver.

bandwidth of interest is a small fraction of the center frequency and, hence, a uniform delay (linear phase) is only required over this narrow bandwidth. One way to implement the delay is to approximate the uniform delay with a constant phase shift inside the signal bandwidth. This makes the carrier phase at different paths coherent, but because of the constant phase shift and, hence, zero group delay, it does not synchronize the baseband modulation signals. As the ratio of signal bandwidth to carrier frequency increases, this baseband time incoherence affects the signal integrity and results in constellation spreading. This signal degradation is independent of the mechanism and/or the architecture used to produce the phase shift. The effect can be best seen through the following example.

Fig. 1 shows the simulated constellation of the received signal (without noise) for an eight-path phased-array receiver at bit rates of 1 and 10 Gb/s at the worst case incident angle of 90° with respect to normal, using a quadrature phase-shift keying (QPSK) modulation scheme with a carrier frequency of 24 GHz. A square-root raised cosine filter with a rolloff factor β of 0.5 is used at both the transmitter and receiver for pulse shaping. A β of 0.5 corresponds to a spectrum efficiency of 1.33 bits/s/Hz.

As the direction of the beam becomes more oblique, the delay between the paths increases and so does the error introduced by constant phase-shift approximation. The constellation spreading is a function of the signal's angle of arrival, ratio of signal bandwidth to the carrier frequency, and the modulation pulse shape. The error vector magnitude (EVM) is a measure of constellation spreading and quantifies the difference between the measured and ideal modulated signals. In a typical receiver, the EVM is degraded due to noise, nonlinearity, and mismatches between in-phase (I) and quadrature-phase (Q) paths. The approximation of propagation delay with a constant phase shift is another factor contributing to a higher EVM in phased-array systems. The EVM of the received signal is calculated for different signal bandwidths and angles of incidence and the result is plotted in Fig. 2. As can be noted, for a carrier of 24 GHz, even for bit rates as high as 1 Gb/s and an incidence angle of 90° (worst case), the level of EVM is lower than 2°, and the signal integrity is maintained without the need for any additional equalization. This figure shows the narrow-band phase-shifting approach to be a viable solution for wireless communications at 24 GHz. Of course, there is a gradual degradation of the constellation integrity as the signal bandwidth continues to increase.

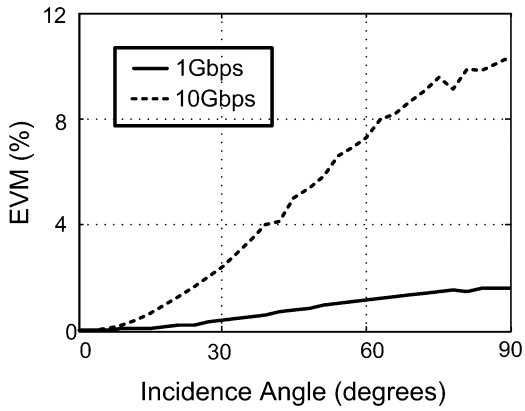

Fig. 2. EVM for two signal bandwidths of 750 MHz (1 Gb/s) and 7.5 GHz (10 Gb/s) in an eight-path narrow-band phased-array receiver at 24 GHz.

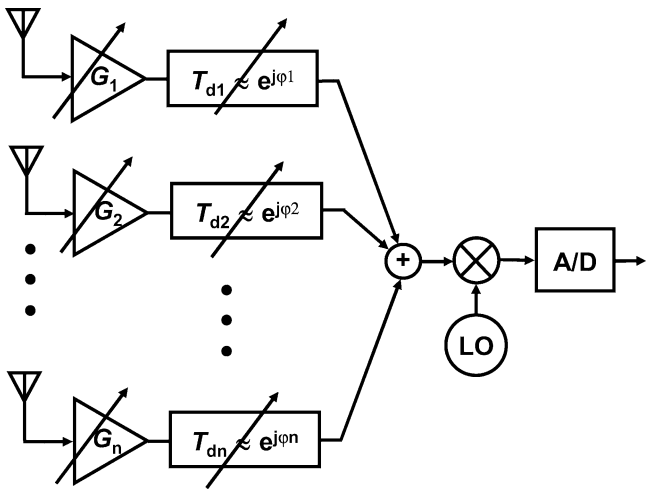

Fig. 3. Simplified scheme of phase shifting at RF in a homodyne receiver.

As mentioned earlier, phase shifting can be performed at different stages, giving rise to different phase-array architectures. These architectural variations will be discussed below.

III. Phased-Array Radio Architectures

A. Signal Path Phase Shifting

The most common method of adjusting the signal time delay T_D is by approximating it with a variable phase shift ϕ_i at the bandwidth of interest in each signal path, as shown in Fig. 3. The phase shifters should have a relatively low loss across the bandwidth of the received signal so that they do not attenuate the received signal and degrade the overall signal-to-noise ratio. A low-loss and broad-band variable phase shifter at high frequencies is a challenging building block to implement in an integrated setting and is a source of active research [10], [11]. By phase shifting and signal combining at RF, other radio blocks are shared among the paths resulting in reduced area and power consumption. Additionally, since the unwanted interference signals are cancelled after signal combining, the dynamic-range (both linearity and noise figure) requirements of the following blocks are more relaxed, allowing them to trade this with other system requirements such as power consumption. If amplitude control

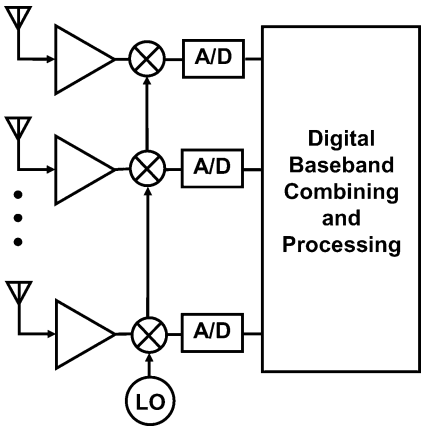

Fig. 4. Simplified scheme of digital-array implementation in a homodyne receiver.

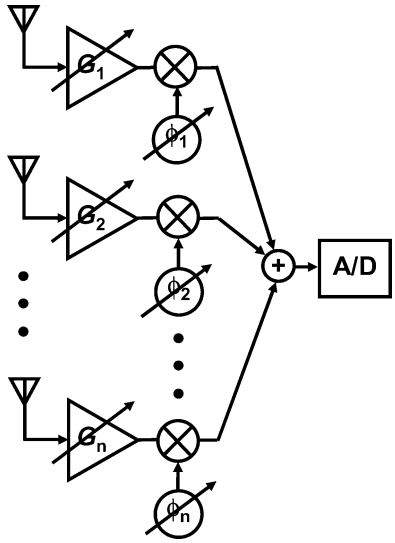

Fig. 5. Simplified scheme of phase shifting at the LO in a homodyne receiver.

is needed (e.g., for null placement), it can be achieved by variable-gain low-noise amplifiers (LNAs) before or after the phase shifters at RF.

Phase shifting and signal combining can also be performed after down-converting the received signals to an IF. Due to the additional signal amplification at the RF stages, phase-shifter loss will have a less deteriorating effect on receiver sensitivity in case it is performed at the IF stage. However, some of the aforementioned advantages, including a lower dynamic-range requirement for the RF mixer, become less effective. Moreover, the value of passive components (e.g., inductors and capacitors) needed to provide a certain phase shift is inversely proportional to the carrier frequency. Since the values of integrated passive components are directly related to their physical size (i.e., area), passive phase shifters at IF consume a larger area compared to the ones at RF.

B. Digital Arrays

The delay and amplitude of the received signal can be adjusted at the baseband using a digital processor (Fig. 4). Digital-array architecture is very flexible and can be adapted for other multiple antenna systems used for spatial diversity such as multiple-input multiple-output (MIMO) schemes [13], [14]. Despite its potential versatility, baseband phased-array architecture uses a larger number of components compared to the previous two approaches, resulting in a larger area and more power consumption. At the same time, since the interference signals are not cancelled before baseband processing, all the circuit blocks, including the power-hungry analog-to-digital converters, need to have a large dynamic range to accommodate all the incoming signals without distortion. Above all, handling and processing a large amount of data through multiple parallel receivers can be challenging even for today's advanced digital technology.

For instance, imagine a digital array of eight receivers where each has a 6-bit analog-to-digital converter that samples the signal with a 10-MHz channel bandwidth at twice the Nyquist rate. These numbers are on the low end of the acceptable range for a typical wireless system. Nevertheless, the baseband data rate of the whole system can be calculated to be 1.92 GB/s. As a comparison, the fastest rate for sending the data into a personal computer using today's peripheral component interconnect (PCI) standard is 32 bits $\times$ 33 MHz $=$ 1.056 Gb/s. This rate is almost halved when notebook computers are used (e.g., the IEEE1394 Standard supports 400 Mb/s). Alternatively, a very powerful digital signal processing (DSP) core can be used to process this large influx of data, but it is going to be bulky, power-hungry, and expensive in today's technology.

In short, until faster and more power-efficient digital data processing becomes available at a lower price, digital implementations still seems to be a more expensive solution for multiple-antenna systems.

C. LO Path Phase Shifting

As an alternative approach, one can indirectly vary the phase of the received signal by adjusting the phase of the LO signal used to down-convert the signal to a lower frequency. This is due to the fact that the output phase of a multiplier (or mixer) is a linear combination of its input phases, i.e.,

$$\begin{aligned} V_{\rm out}(t) &= \cos(\omega_{\rm RF}t+\phi_{\rm RF}) \times \cos(\omega_{\rm LO}t+\phi_{\rm LO}) \\ &= \frac{1}{2}\cos\left[(\omega_{\rm RF}\pm\omega_{\rm LO})t+(\phi_{\rm RF}\pm\phi_{\rm LO})\right]. \end{aligned} \quad (2)$$

Fig. 5 shows a simplified phase-array receiver that uses LO phase shifting. Phase shifting at the LO port is advantageous in that the phase-shifter loss does not directly deteriorate the receiver sensitivity. Additionally, the nonlinearity and loss of active phase shifters such as phase-interpolating implementations (e.g., [12]) can be more easily tolerated in the LO path compared to the signal path. However, since the undesired interferences are only rejected after the combining step at the IF, the RF amplifiers and mixers need to have a higher dynamic range than the ones in the signal-path phase-shifting scheme. The signal amplitude can be controlled using RF or IF variable-gain amplifiers (VGAs).

This architecture is particularly attractive for silicon-based integrated systems due to the large number of transistors available

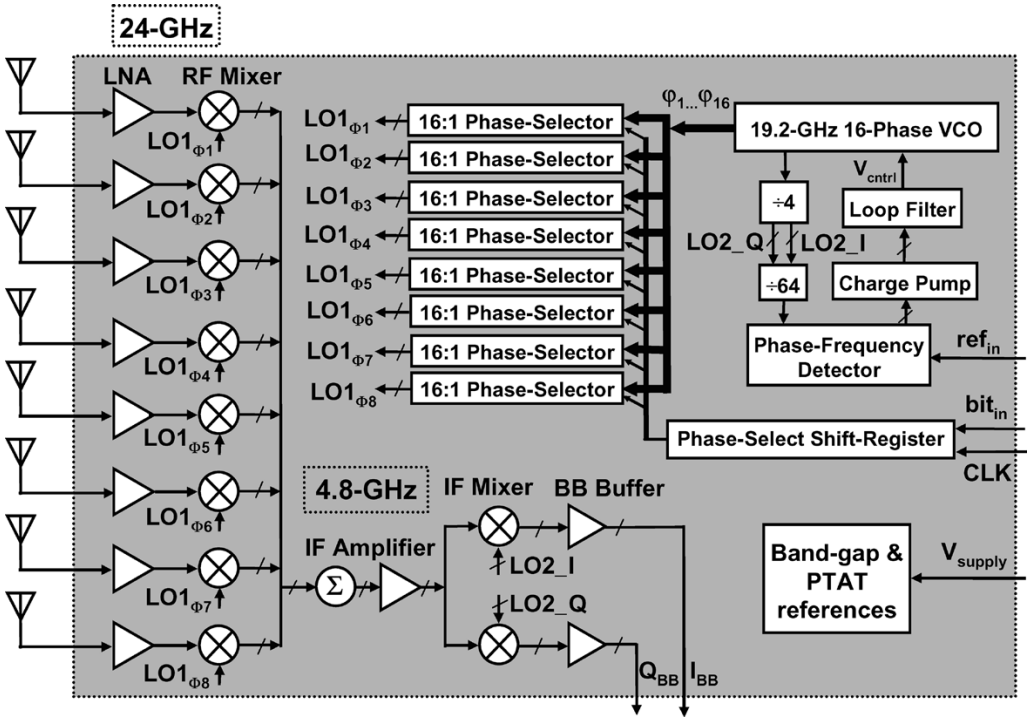

Fig. 6. Block diagram of the fully integrated 24-GHz phased-array receiver.

and the possibility of accurate multiple phase generation and distribution, which will be discussed in great details below.

IV. 24-GHz Phased-Array Receiver Architecture

The implemented phased-array receiver employs an LO phase-shifting architecture for several reasons. Phase shifting and signal processing at baseband (i.e., digital arrays) was eliminated due to the larger chip area, power consumption, and the high demand on the baseband digital interface, particularly for the high data rates of interest.

Passive variable phase shifters at 24-GHz RF will have a relatively higher loss due to ohmic and silicon substrate loss in integrated passive components (especially inductors and varactors). This loss in the signal path deteriorates the receiver's overall sensitivity and can be minimized by providing more gain at the LNA preceding them. More importantly, the phase-shifter's loss usually changes significantly with its phase shift that necessitates the use of RF VGAs with fine resolution to compensate these variations. Additionally, phase-shifter nonlinearity will be directly in the signal path, making the receiver more sensitive to a strong blocker.

In contrast, the signal loss in the LO phase-shifting networks can be easily compensated by high-gain amplifiers (e.g., limiters) without the need for any amplitude tuning. The reason for this is that many RF mixer implementations (e.g., Gilbert type) perform better when driven to switch with a large amplitude at the LO port making their conversion gain less sensitive to the LO amplitude. This approach also makes it possible to generate multiple phases of an LO signal by efficient methods other than using phase shifters.

The aforementioned considerations led to the design of a phased-array receiver that uses different phases at the LO path. The block-diagram schematics of the 24-GHz phased-array receiver consisting of eight paths is shown in Fig. 6. The receiver uses a two-step down-conversion architecture with an IF of 4.8 GHz for two main reasons. Firstly, compared to single down-conversion schemes such as homodyne, a heterodyne-type receiver achieves more selectivity and gain control at multiple stages. Secondly, with the mentioned frequency planning, both LO frequencies can be generated in one synthesizer loop with the use of a divide-by-four block, as shown in the upper right part of Fig. 6.

A single oscillator core generates 16 discrete phases (i.e., 4-bit resolution) that are used to control the phase of each path. The effect of using discrete phase compensation is discussed in Section V. A set of eight phase selectors (i.e., analog phase multiplexer) provides the appropriate phase of the LO to the corresponding RF mixer for each path *independently*. In other words, the LO phase for each path can be chosen irrespective of the phase of the other paths. The phase-selection data is serially loaded to an on-chip shift register using a computer interface.

The image frequency of the first down-conversion at 14.4 GHz is attenuated by the narrow-band transfer function of the front-end (i.e., antenna and LNA). Since communication schemes around the image-frequency band are mainly low power, and due to the directionality of the phased-array receiver, no additional image-rejection provisions are introduced. The final down-conversion to baseband or very low-IF is done by a pair of quadrature mixers. The divide-by-four block that is used to generate the second LO will naturally produce I and Q signals to drive these mixers.

Each RF path consists of two stages of low-noise amplification and a down-conversion mixer. The design of the 24-GHz front-end and receiver signal path is discussed in [9]. In Section V, multiple phase generation and distribution of the 19-GHz LO are described in detail.

V. Multiple Phase Generation and Distribution

A. Quantized Phase Effects

An on-chip LO generates 16 discrete phases of the LO that can either be directly applied to the RF mixers or interpolated between to generate additional intermediate phases in order to compensate the narrow-band phase shift of the carrier frequency at each path. This discrete method can only compensate the carrier phase shift at a few incidence angles *precisely*. For all other angles, the signal constellation at each received path is rotated with an amount equal to the value of phase quantization error. Clearly, the phase quantization error depends on the desired phase shift for each path, itself a function of the angle of incidence. Since the constellation at each received path is rotated differently, the combined signals are not added coherently, causing interference between the I and Q channels.

Fig. 7 plots the EVM as a function of the angle of incidence when discrete phase shifts are used at the receiver for 8 (3 bit), 16 (4 bit), and 32 (5 bit) equally spaced phases. The signal has a bandwidth of 7.5 GHz and all the other simulation parameters are identical to the ones described in Section II. Using a 4-bit phase-shifting scheme with phase steps of 22.5° creates a peak EVM at an incidence angle of 70°, which is 1.5 times larger than the peak EVM generated if an LO with a continuous phase shift was available. For continuously adjustable phase shift, the peak naturally happens at an incidence angle of 90°, which corresponds to largest time delay between antennas. As a comparison, if a 3-bit phase shifting scheme with 45° phase steps was used, this peak occurs at incidence angle of 60° with a peak EVM value, which is 1.8 times the peak EVM value for a 4-bit scheme. The ratio of these peaks depends on the bandwidth of signal, and tends to increase for lower signal bandwidths.

In Fig. 8, we show that using discrete LO phases does not sacrifice the beam-forming accuracy significantly. In fact, in the worst case, the signal loss is less than 1 dB in this 4-bit phase-shifting scheme for a full spatial coverage.

B. Multiple Phase Generation

At least two distinct methods to create various phases of an LO signal can be envisioned. In the first approach, only one phase is generated in the oscillator core (two phases considering differential signals). Phase shifters, phase interpolators, or similar blocks follow the oscillator in order to generate multiple phases of its output signal in a continuous or discrete fashion [12], [15]. These blocks can be narrow-band around the LO frequency and their loss is usually not a major concern in the LO path. In the second scheme, multiple phases are generated inside the oscillator core. Usually, this method results in discrete phases with a minimum resolution of $2\pi/N$, where N is an integer number.

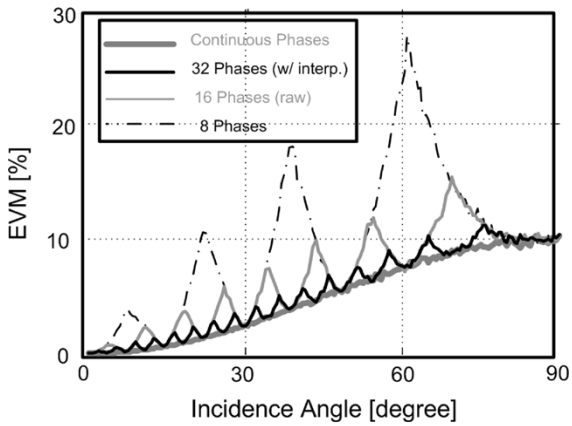

Fig. 7. EVM for continuous-phase 5-bit (one-step interpolation), 4-bit (raw resolution), and 3-bit (hypothetical) phase-shifting resolutions.

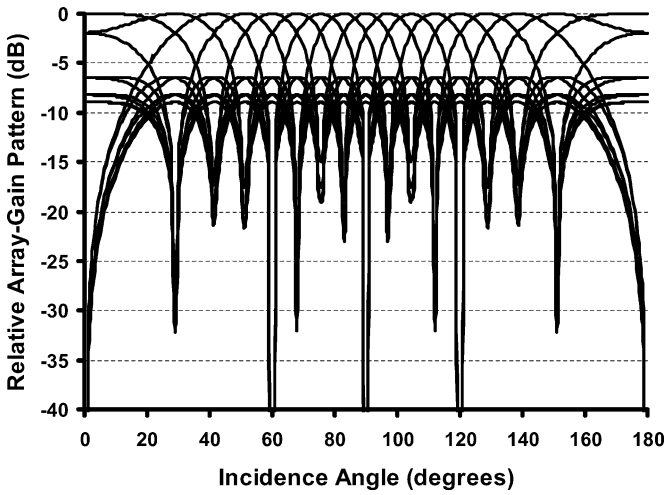

Fig. 8. Array pattern with 4-bit phase-shifting resolution.

In our design, a ring connection of eight fully differential CMOS amplifiers forms the 19.2-GHz voltage-controlled oscillator (VCO) capable of generating 16 phases (Fig. 9) [16]. By flipping one of the connections, the number of amplifying stages is cut into half in a fully differential structure (top left connection of Fig. 9). These phases are then applied to phase selectors that can also function as interpolators generating a finer phase resolution.

If no inductors at the amplifier outputs were used (e.g., differential pair with resistive load or CMOS inverters), each amplifier should have operated at a speed very close to the maximum operating frequency of transistors in the process causing challenges for a reliable startup. To better observe this, imagine that each amplifier could be modeled as a single-pole system

$$H(s) = \frac{A_0}{1 + \dfrac{s}{s_0}}, \qquad s = j\omega. \tag{3}$$

Each amplifier could produce a phase shift equal to $\tan^{-1}(\omega/\omega_0)$. In the case of a 22.5° phase shift for each amplifier at 19 GHz, the pole frequency should be at least at 46 GHz. Since the gain of each stage should be more than one to guarantee oscillation startup, the unity-gain frequency of each amplifier ($\approx A_0 \cdot \omega_0$) approaches the device cutoff

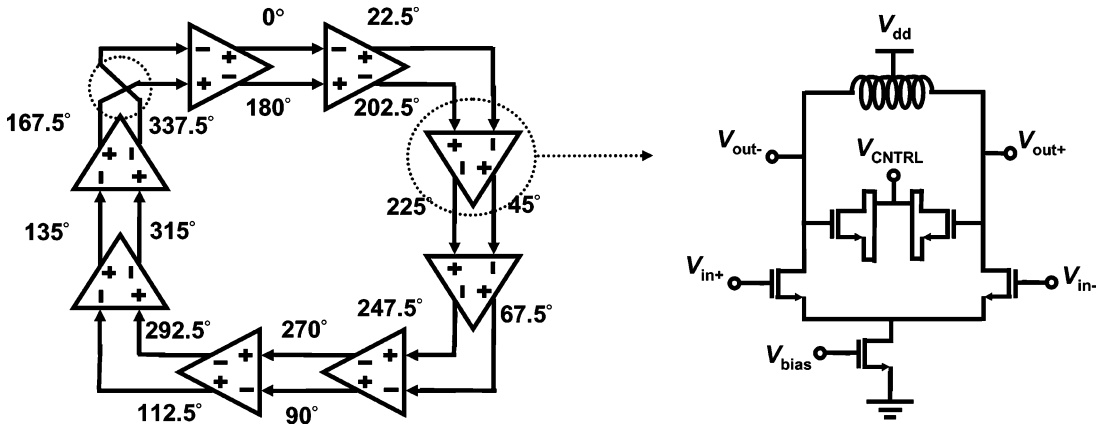

Fig. 9. Schematic of the 16-phase 19.2-GHz CMOS ring VCO.

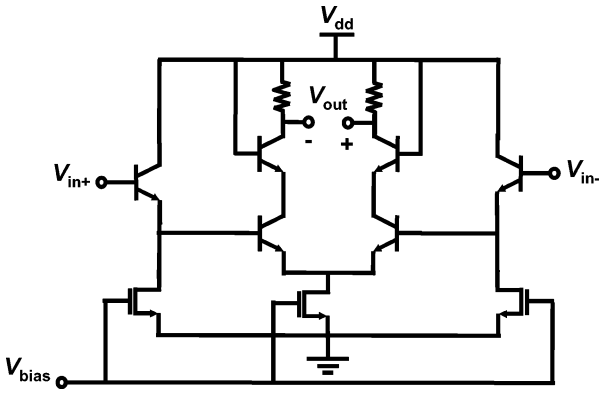

Fig. 10. Schematic of the VCO buffer.

frequency. Unfortunately, this imposes unnecessary restrictions on the individual transistor's speed and current consumption.

However, inductors can generate the necessary phase shift for each amplifier in the following fashion. At the oscillation frequency $\omega_{\rm osc}$, the equivalent parallel RLC load causes a phase shift of

$$\Delta\Phi = \frac{\pi}{2} - \tan^{-1}\frac{L\omega_{\rm osc}}{R\left(1 - LC\omega_{\rm osc}^2\right)}. \tag{4}$$

In the case of a 22.5° phase shift for each stage, we should have

$$LC = \frac{1}{\omega_{\rm osc}^2}\left(1 - \frac{1}{Q \cdot \tan 3\pi/8}\right) \tag{5}$$

where Q is the load quality factor and is equal to $R/L\cdot\omega_{\rm osc}$. For $Q \approx 15$ at 19 GHz in this process, $LC \approx 0.97/\omega_{\rm osc}^2$ or $\omega_{\rm osc} \approx 0.99/\sqrt{\rm LC}$. In other words, each amplifier is almost tuned at the oscillation frequency. Each of the designed amplifier stages draws less than 3.2 mA from a 2.5-V supply resulting in a total power consumption of 63 mW for the oscillator.

The center frequency can be tuned by changing the control voltage of differential MOS varactors. In order to make the high-frequency oscillator insensitive to loading, all the eight differential outputs are buffered prior to connection to other circuit blocks (Fig. 10). Emitter followers and differential pairs draw approximately 1 and 1.9 mA from a 2.5-V supply, respectively. This results in approximately 9.8 mW of power consumption for each buffer.

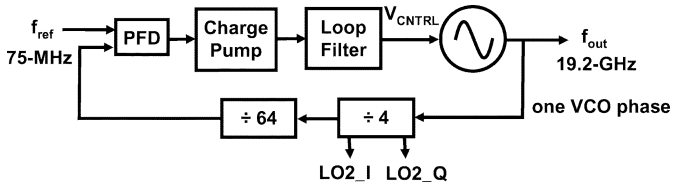

Fig. 11. Schematic of the third-order PLL.

An on-chip third-order phased-locked loop (PLL) with a loop bandwidth of 7 MHz is designed to lock the 19.2-GHz LO signal to a 75-MHz external reference signal source (Fig. 11). The integrated synthesizer uses a standard tri-state frequency phase detector [22] and a multiswitch charge pump [17] to minimize the reference feed-through. All divide-by-two blocks use a master–slave architecture and an emitter coupled logic for high-speed operation (Fig. 12).

In order not to disturb the symmetry of VCO output phases, none of them are connected to any external pads for measurements. Nevertheless, we can verify the standalone VCO performance by picking up the high-frequency signal via a loop antenna placed on top of the chip.

The frequency of the VCO can be continuously varied from 18.8 GHz to 21 GHz (Fig. 13). The slope of this transfer characteristic is 2.1 GHz/V at 19.2 GHz and reaches a maximum of 2.67 GHz/V close to 19.6 GHz.

The output spectrum and phase noise of the VCO at 18.70 GHz is shown in Fig. 14. The VCO achieves a phase noise of −103 dBc/Hz at 1-MHz offset from the carrier. The measurement at higher offset frequencies is limited by the thermal noise floor of the spectrum analyzer used to measure the phase noise.

The output spectrum and phase noise of the locked VCO are shown in Fig. 15. As can be seen, the phase noise stays constant within the loop bandwidth as the frequency changes. Our synthesizer phase-noise measurements have been limited by the phase noise of a synthesized sweeper that was used as the 75-MHz input reference signal. Better phase noise is expected if a crystal type reference is used.

C. Systematic Phase Distribution

It is essential that the 16 generated phases of the VCO are fed to each of the eight phase selectors in Fig. 6 with equal

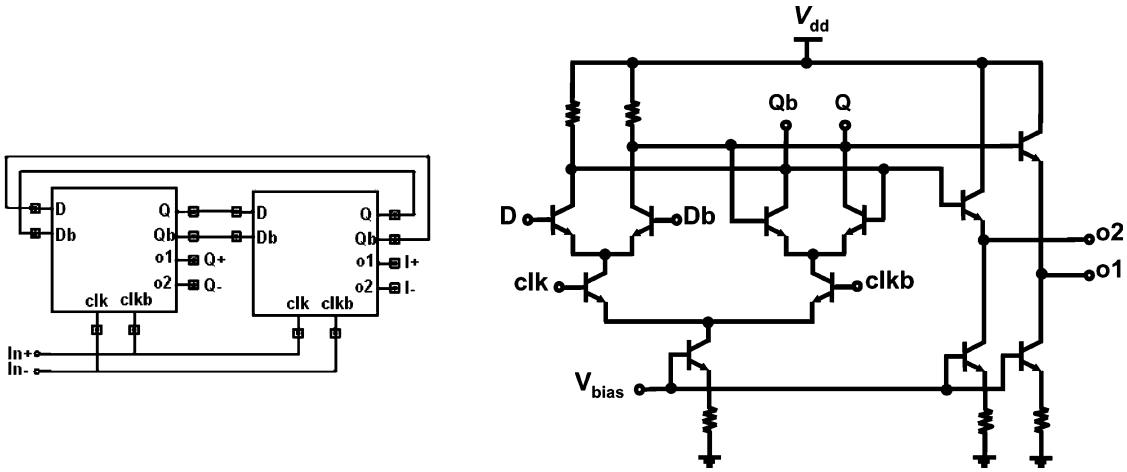

Fig. 12. Schematic of the high-speed divide-by-two blocks.

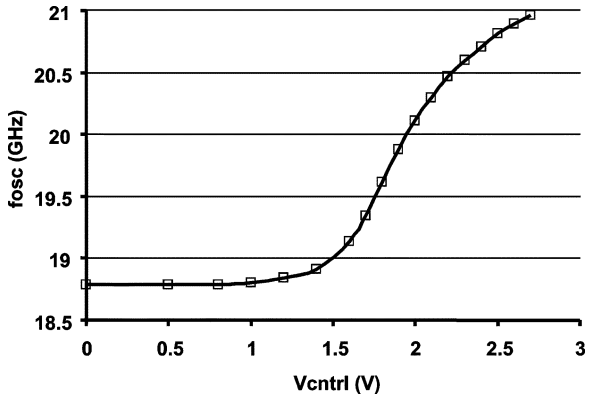

Fig. 13. VCO frequency versus control voltage.

amplitudes and delays. A symmetric binary tree structure, as shown in Fig. 16(a), is used to distribute LO phases. Each path consists of 16 metal lines running in parallel, similar to Fig. 16(b).

Due to the strong EM coupling between the closely spaced metal lines, the symmetry not only depends on the path length, but also on the phase arrangement within the bus due to EM coupling between the lines. Several mechanisms, such as multimode excitation, coupling between nonadjacent lines, and boundary discontinuity of a finite array can cause phase and amplitude mismatches in the tree structures of Fig. 16(a) and (b). To understand the multimode excitation, consider two identical lossless transmission lines T_1 and T_2 running in parallel and driven by two signal sources V_o and $V_o e^{j\theta}$, respectively. If $\theta = 0^\circ$ (even-mode excitation), the characteristic impedance of each line is given by

$$Z_{\text{even}} = \sqrt{\frac{l + l_m}{c}} \tag{6}$$

where c, l, and l_m are per-unit-length capacitance to ground, inductance, and mutual inductance, respectively. On the other hand, for a $\theta = 180^\circ$ (odd-mode excitation), the characteristic impedance of each line is given by

$$Z_{\text{odd}} = \sqrt{\frac{l - l_m}{c + 2c_m}} \tag{7}$$

where c_m is the per-unit-length coupling capacitance to the adjacent line. In general, the traveling wave can be considered as a linear combination of even- and odd-mode transmissions. Let Z_{o1} and Z_{o2} denote the characteristic impedances of T_1 and T_2, respectively. The magnitude and phase of Z_{o1} and Z_{o2} are related to phase difference θ by

$$\begin{aligned} |Z_{o1}| &= |Z_{o2}| \\ &= \frac{\sqrt{2} Z_{\text{even}} Z_{\text{odd}}}{\sqrt{Z_{\text{odd}}^2 (1 + \cos\theta) + Z_{\text{even}}^2 (1 - \cos\theta)}} \end{aligned} \tag{8}$$

$$\begin{aligned} \angle Z_{o1} &= -\angle Z_{o2} \\ &= \arctan \frac{Z_{\text{even}} \sin\theta - Z_{\text{odd}} \sin\theta}{Z_{\text{odd}}(1 + \cos\theta) + Z_{\text{even}}(1 - \cos\theta)}. \end{aligned} \tag{9}$$

It can be seen that Z_{o1} and Z_{o2} form a complex conjugate pair, which are equal only for $\theta = 0^\circ$ or 180°.

EM crosstalk between nonadjacent lines can also cause phase and amplitude errors [19]. EM simulations are performed on an array of 16 on-chip transmission lines, as shown in Fig. 16(b). In our design, each line is 4-μm thick, 5-μm wide, and 200-μm long with a 5-μm edge-to-edge spacing. These lines are 12 μm above the silicon substrate. Fig. 17 shows the extracted mutual inductance and coupling capacitance normalized to the inductance l and capacitance c, respectively. It illustrates that although the capacitive coupling is negligible between nonadjacent lines, the magnetic coupling is significant and the mutual inductance decreases very slowly with the distance.

Fig. 16(b) shows three different phase arrangements in a transmission-line bus carrying multiple phases. If the array has an infinite number of lines, arrangement 1 provides the best symmetry, and the characteristic impedance can be calculated to be

$$Z_o = \sqrt{\frac{l + 2\sum_{k=1}^{\infty} l_{mk} \cos k\theta}{c + 2\sum_{k=1}^{\infty} c_{mk}(1 - \cos k\theta)}} \tag{10}$$

where l_{mk} and c_{mk} are the mutual inductance and coupling capacitance between two lines with phase difference of $k\theta$.

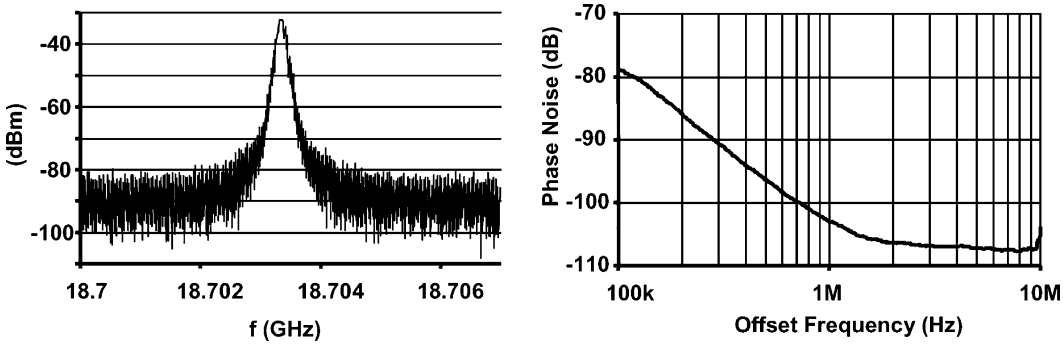

Fig. 14. VCO output spectrum and phase noise at 18.7 GHz.

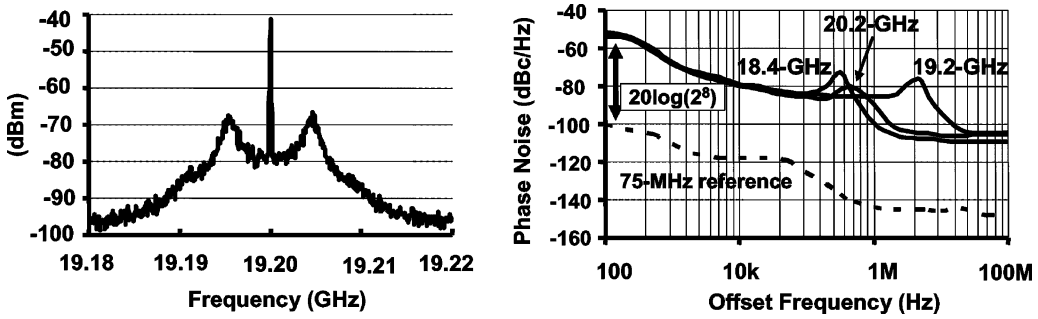

Fig. 15. Output spectrum and phase noise of the locked VCO.

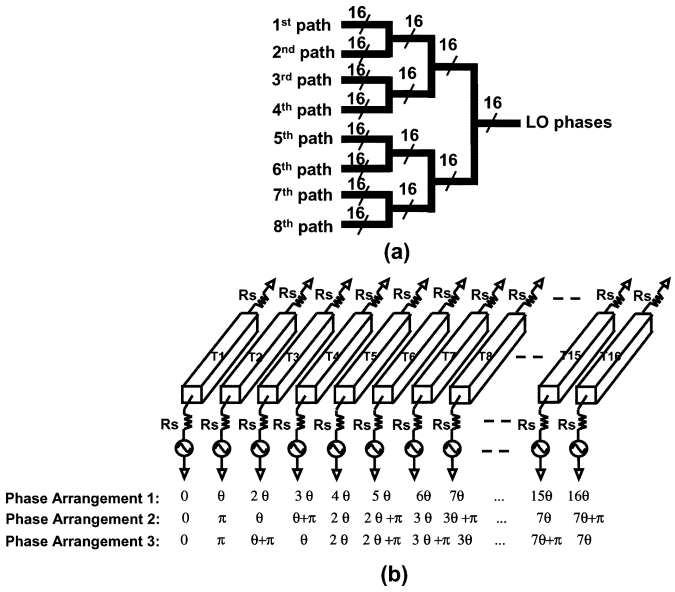

Fig. 16. (a) LO phase distribution tree structure. (b) Phased transmission-line array.

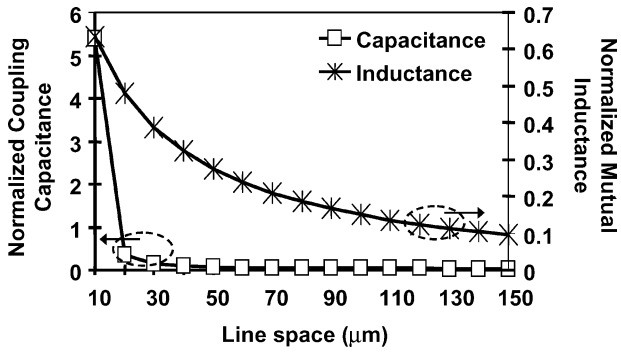

Fig. 17. Simulated coupling capacitor and inductor of the phase distribution line array of Fig. 16.

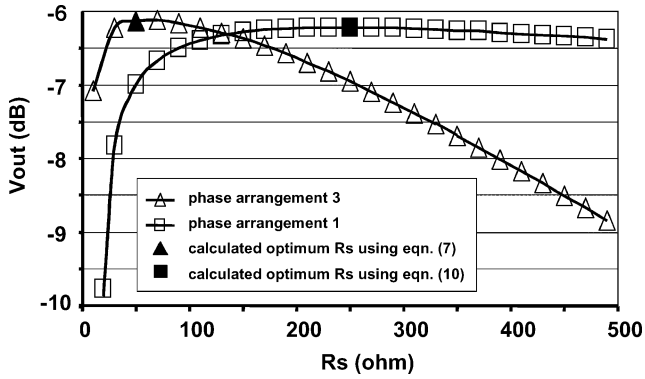

Fig. 18. Output voltage of the phase distribution line versus the source impedance value.

However, in a finite array, the discontinuity at the edge and the inductive crosstalk between nonadjacent lines can produce significant mismatch at the outputs of arrangement 1.

According to Ampere's law, placing differential phase pairs as shown in arrangements 2 and 3 can minimize magnetic coupling. If θ is small (in this study, $\theta = 22.5°$), arrangement 3 has better phase- and amplitude-matching characteristics than the other two. This is because, in arrangement 3, the adjacent lines of two different pairs are closer in phase so that the capacitive coupling between them is minimized. For a small θ, the characteristic impedance of the transmission lines in arrangement 3 can be approximated by the odd-mode impedance given by (7).

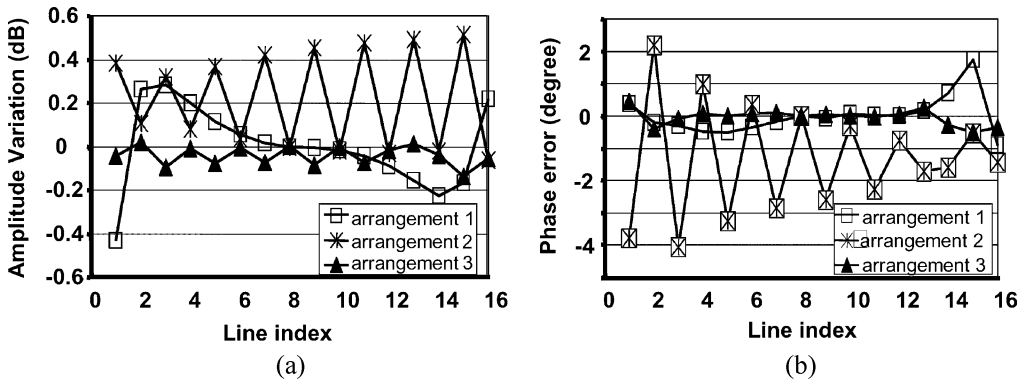

Fig. 19. Comparison of different phase distribution configurations of Fig. 16(b). (a) Amplitude matching. (b) Phase matching.

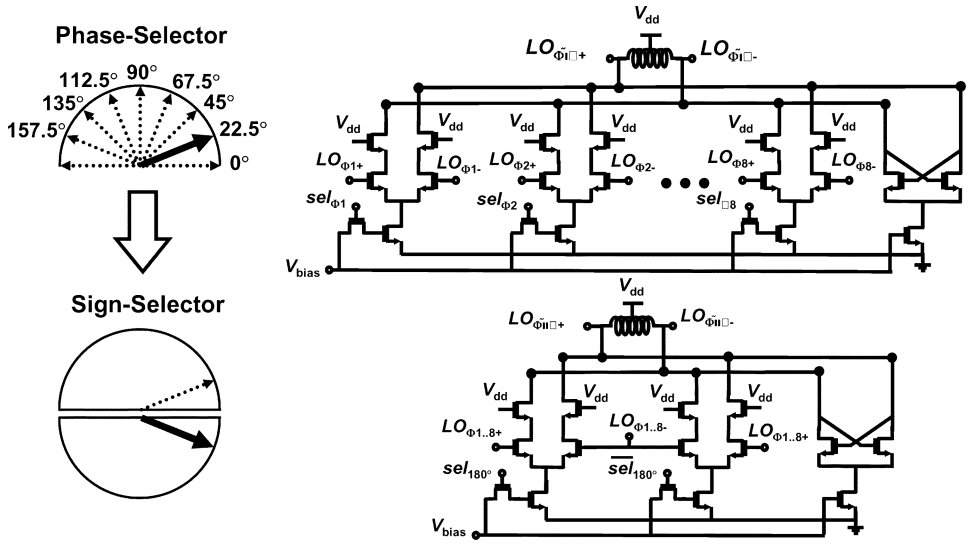

Fig. 20. Phase-selection circuitry.

To compare these three proposed phase arrangements, EM simulations were performed. Each of the three arrays is driven by 16 evenly spaced phases of a 19.2-GHz sinusoid. The transmission lines see a resistance R_s at both input and output ports. Fig. 18 illustrates the voltage at the output port of the central wire as a function of R_s. It verifies that using resistance values estimated by (10) and (7) results in maximum $V_{\rm out}$ for arrangements 1 and 3, respectively. Fig. 19(a) and (b) shows the magnitudes and phases of the voltages at the 16 output ports for three arrangements. It can be seen that arrangement 3 exhibits less mismatch and, hence, is adopted in our 24-GHz phased-array receiver.

The LO phase distribution lines transform the input impedance of the phase-selection circuitry to a new impedance at the LO buffer output node of Fig. 9. This transformed impedance should be made equal to the complex conjugate of the output impedance of the LO buffer to achieve the maximum power transfer and, hence, the largest LO amplitude at the input of phase-selection circuitry. Under a conjugate matched condition and neglecting the loss in distribution lines, the theoretical maximum achievable differential signal swing at the input of each phase-selection circuitry is

$$V_{\rm diff} = \frac{1}{2\sqrt{n}} i_{\rm bias} \sqrt{R_{\rm out} R_{\rm in}} \tag{11}$$

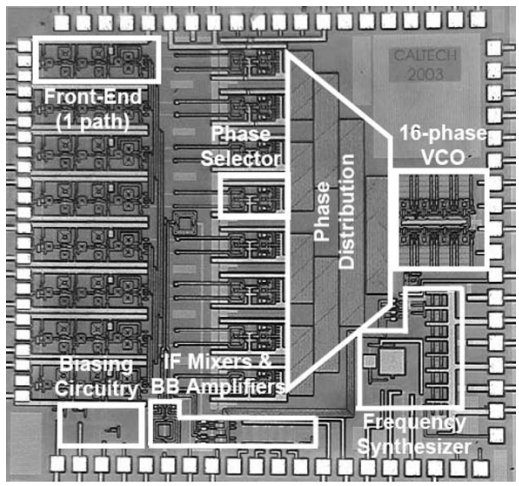

Fig. 21. Die microphotograph.

where $i_{\rm bias}$ and $R_{\rm out}$ are the tail current and output resistance of the differential-pair buffer in Fig. 9, respectively; $R_{\rm in}$ is the input resistance of each phase selector and $n = 8$ is the number of phase selectors that are connected to a single LO buffer. In our implementation, the maximum swing based on (11) is approximately 140 mV. Due to the inaccuracies in prediction and

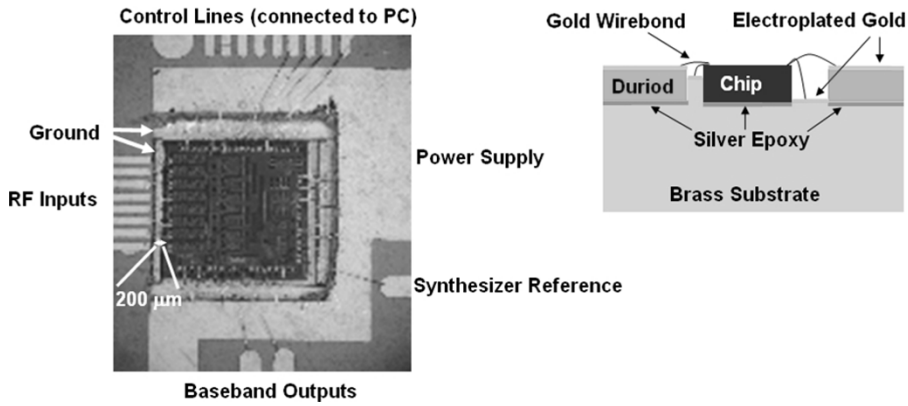

Fig. 22. High-frequency measurement setup.

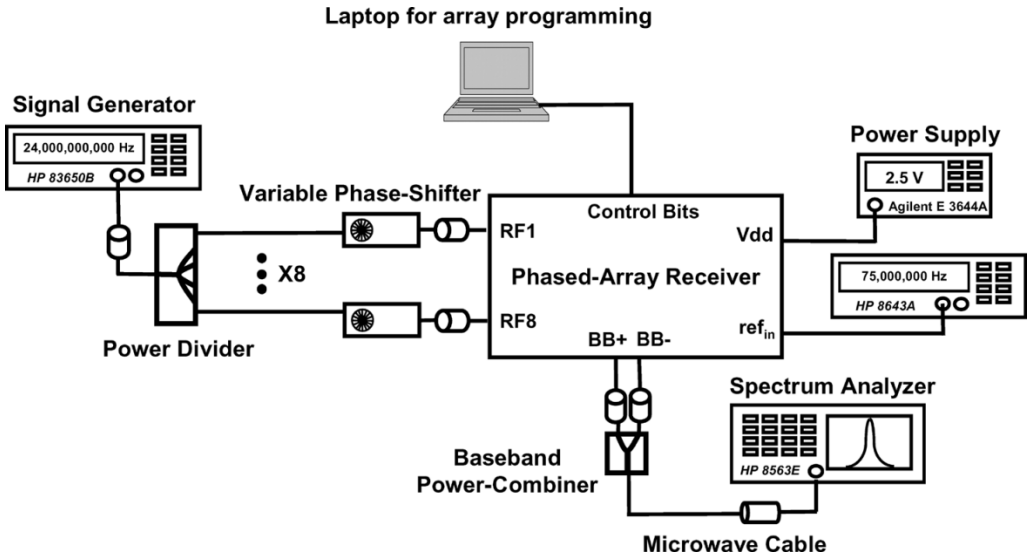

Fig. 23. Array measurement setup.

modeling of LO distribution lines in addition to their loss at 19 GHz, we expect the amplitude to be smaller in practice. However, the phase-selection circuitry discussed below is designed to maintain the required LO amplitude across RF mixers.

D. Phase Selector/Interpolator

As previously mentioned, each receiver path has independent access to all 16 phases of the LO. In order to minimize the complexity of the phase-selection circuitry, the appropriate phase of the LO for each path is selected in two steps. Initially, an array of eight differential pairs with switchable current sources and a shared tuned load are used to select one of the eight output pairs of oscillator (Fig. 20). A dummy array with complementary switching signals is used to maintain a constant load and prevent relative changes in phases while switching. In the basic mode of operation, at any given time, one of the LO phases is fed to the output of the main analog multiplexer, while other phases are fed to the output of the unused multiplexer. In the next step, another pair of cross-coupled differential pairs selects the sign bit, resulting in complete access to all LO 16 phases. The above-mentioned cascaded configuration reduces the necessary number of phase selectors (i.e., differential pairs in our case) from 2^4 to 2^3+2 for each path. The cross-coupled differential pairs at the output of each stage partially cancel the loss associated with the inductors and transistors' outputs and, hence, increase the LO amplitude driving RF mixers.

Phase interpolation can be achieved by turning on more than one tail transistor at any given time, forcing the output to be the vector sum of all the turned-on phases. A first-order interpolation can be achieved by turning two adjacent paths on simultaneously, doubling the phase resolution.

VI. Receiver Measurement Results

The phased-array receiver is implemented in an IBM 7HP SiGe BICMOS process with an HBT f_T of 120 GHz and 0.18-μm CMOS transistor [20]. The die micrograph of the chip is shown in Fig. 21. The chip occupies an area of 3.3 mm $\times$ 3.5 mm.

For all measurements, the silicon chip has been mounted on a gold-plated brass substrate to provide a good grounding. A high-frequency Duroid board surrounds the chip and is used to connect the input, bias, and control signal lines using wire bonds (Fig. 22). Special attention has been paid to minimize the length of wire bonds at RF input and ground lines. All signal and bias lines are fed with standard subminiature A (SMA) connectors attached to the brass membrane.

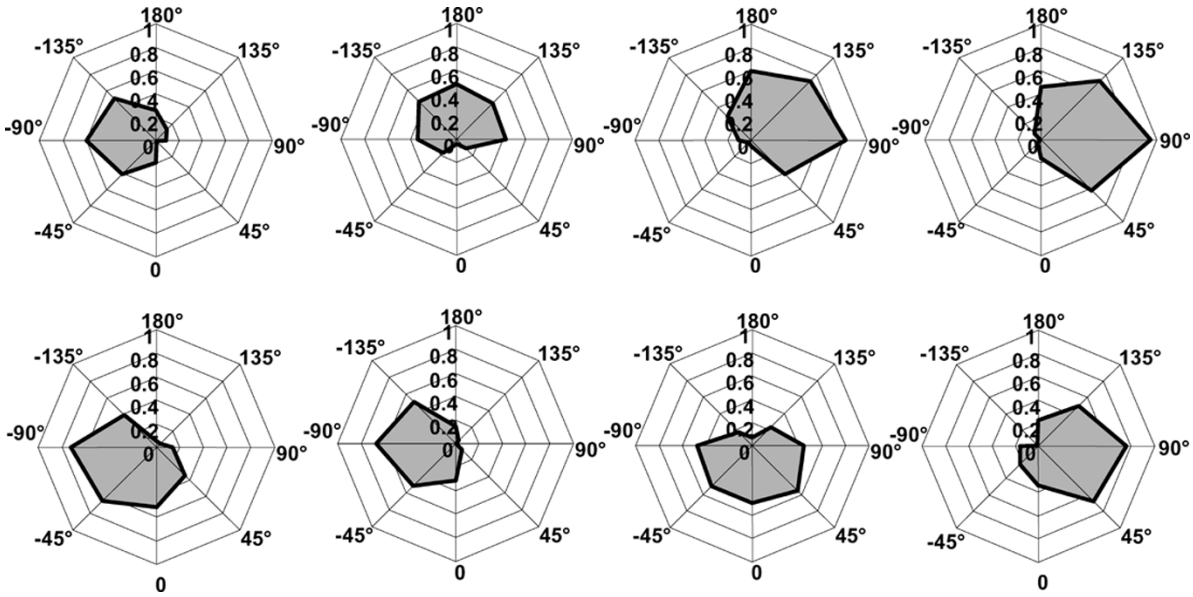

Fig. 24. Measured array patterns with two operating paths.

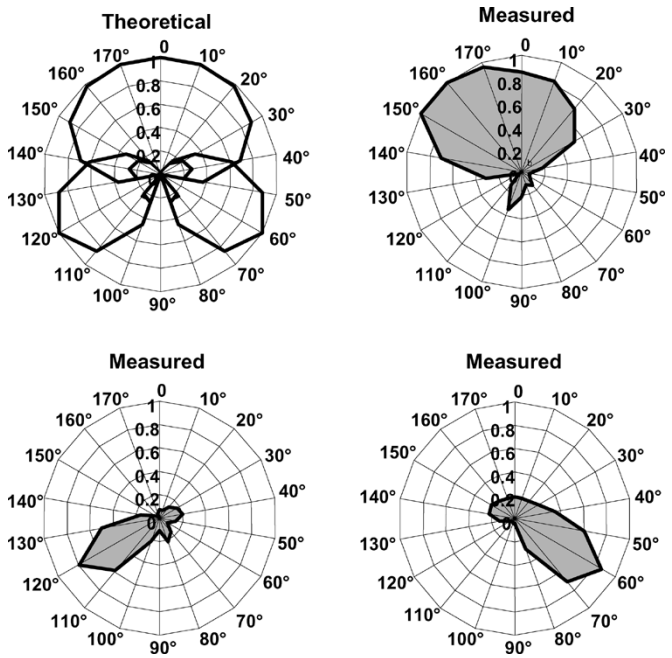

Fig. 25. Measured array pattern with four operating paths.

TABLE I
SUMMARY OF THE MEASURED PERFORMANCE

Signal Path Performance (per path)*	
Peak Gain	43dB
Noise-Figure	7.4dB
Input-Referred 1dB Compression Point	-27dBm
Input-Referred 3rd-Order Intercept Point	-11.5dBm(2 tones 5MHz apart)
On-chip Image Rejection	35dB
Current Consumption [*RF (each path) / IF*]	12mA/12mA
S_{11}	< -10dB
LO Path Performance	
Synthesizer Locking Range	2GHz (10%)
Synthesizer Bandwidth	7MHz
VCO Phase Noise	-103dBc/Hz @ 1MHz offset
Current Consumption (VCO + buffers)	59mA
Complete Receiver Performance (8 paths)	
Total Array Gain	61dB
SNR Improvement	9dB
Phase-shifting Resolution	4 bits
Beam-forming Peak-to-Null Ratio	20dB (measured for 4 paths)
Current Consumption @ 2.5V	364mA
	287mA (w/o biasing and baseband buffers)
Technology	SiGe, 120GHz HBT, 0.18μm CMOS
Die Area	3.5mm x 3.3mm

*RF to baseband

Ideally, all the input paths have to be connected to on-board antennas [4] and the reception pattern of the array has to be measured. However, in order to separate the effect of the antenna array from the receiver, phase shifters in the input path are used to emulate the phase difference of signals at each path. Array measurements have been performed with a signal being fed to only four of the receiver paths. The setup used for array measurements is shown in Fig. 23.

Receiver pattern measurements at eight different angles with only two operating paths are shown in Fig. 24. The difference between the peak and the null is 10–20 dB in all cases. This value is mostly limited by the mismatch in different paths and can be significantly improved with a gain control block in each receiver path for future implementations. In any event, using all eight paths is expected to significantly improve this number, as well as make the beamwidth narrower. Theoretical receiver patterns and the measurements at three different angles are shown in Fig. 25 for a four-channel setup.

Table I summarizes the measurement results.

VII. CONCLUSION

Moore's 1965 seminal paper [21] ends with the following prediction: "It is difficult to predict at the present time just how extensive the invasion of the microwave area by integrated electronics will be. . .. The successful realization of such items such

as *phased-array antennas*, for example, using a multiplicity of integrated microwave power sources, could completely revolutionize radar." In this paper, almost 40 years later, we have demonstrated the first silicon-based fully integrated phased-array receiver at microwave frequencies for use in ultrahigh-speed wireless communication and radar applications.

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REFERENCES

[1] "Code of federal regulations, title 47–telecommunication, chapter I," Federal Commun. Commission, pt. 15—Radio Frequency Devices, secs. 15.245 and 15.249, 2004.

[2] "Code of federal regulations, title 47–telecommunication, chapter I," Federal Commun. Commission, pt. 15—Radio Frequency Devices, secs. 15.515 and 15.521, 2004.

[3] H. Hashemi, X. Guan, and A. Hajimiri, "A fully integrated 24 GHz 8-path phased-array receiver in silicon," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2004, pp. 390–391.

[4] D. Lu, D. Rutledge, M. Kovacevic, and J. Hacker, "A 24 GHz patch array with a power amplifier/low-noise amplifier MMIC," *Int. J. Infrared Millim. Waves*, vol. 23, pp. 693–704, May 2002.

[5] X. Guan and A. Hajimiri, "A 24 GHz CMOS front-end," in *Eur. Solid-State Circuits Conf. Tech. Dig.*, Sept. 2002, pp. 155–158.

[6] E. Sonmez, A. Trasser, K. Schad, R. Abele, and H. Schumacher, "A single chip 24 GHz receiver front-end using a commercially available SiGe HBT foundry process," in *IEEE Radio Frequency Integrated Circuits Symp. Dig.*, Jun. 2002, pp. 159–162.

[7] I. Gresham, A. Jenkins, R. Egri, C. Eswarappa, F. Kolak, R. Wohlert, J. Bennett, and J. Lanteri, "Ultra wide band 24 GHz automotive radar front-end," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2003, pp. 369–372.

[8] D. Lu and D. Rutledge, "Investigation of indoor radio channel from 2.4 GHz to 24 GHz," in *IEEE AP-S Int. Symp. Dig.*, Jun. 2003, pp. 134–137.

[9] X. Guan, H. Hashemi, and A. Hajimiri, "A fully integrated 24-GHz 8-path phased-array receiver in silicon," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[10] D. Parker and D. Zimmermann, "Phased-arrays—Part II: Implementations, applications, and future trends," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 3, pp. 688–698, Mar. 2002.

[11] H. Zarei and D. Allstot, "A low-loss phase shifter in 180 nm CMOS for multiple-antenna receivers," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2004, pp. 392–393.

[12] M. Chua and K. Martin, "1 GHz programmable analog phase shifter for adaptive antennas," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1998, pp. 11–14.

[13] T. Rappaport, *Wireless Communications: Principles and Practice*. Upper Saddle River, NJ: Prentice-Hall, 1996.

[14] T. Alamouti, "A simple transmit diversity technique for wireless communications," *IEEE J. Sel. Area Commun.*, vol. 16, no. 8, pp. 1451–1458, Oct. 1998.

[15] T. Yamaji, D. Kurose, O. Watanabe, S. Obayashi, and T. Itakura, "A four-input beam-forming downconverter for adaptive antennas," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1619–1625, Oct. 2003.

[16] J. Savoj and B. Razavi, "A 10-Gb/s CMOS clock and data recovery circuit with a half-rate binary phase-frequency detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13–21, Jan. 2003.

[17] J. Craninckx and M. Steyaert, *Wireless CMOS Frequency Synthesizer Design*. Norwell, MA: Kluwer, 1998.

[18] D. Ham, "Statistical electronics—Noise processes in integrated communication systems," Ph.D. dissertation, Dept. Elect. Eng., California Inst. Technol., Pasadena, CA, 2002.

[19] C.-K. Cheng *et al.*, *Interconnect Analysis and Synthesis*. New York: Wiley, 2000.

[20] A. Joseph *et al.*, "A 0.18 μm BiCMOS technology featuring 120/100 GHz (ft/f_{max}) HBT and ASIC-compatible CMOS using copper interconnect," in *Proc. IEEE Bipolar/BiCMOS Circuits Technology Meeting*, 2001, pp. 143–146.

[21] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[22] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.

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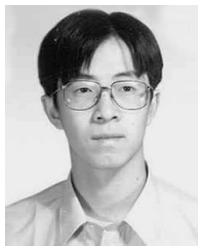

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