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Low Voltage Nanoelectromechanical Switches Based on Silicon Carbide Nanowires

X. L. Feng,[†] M. H. Matheny,[†] C. A. Zorman,[‡] M. Mehregany,[‡] and M. L. Roukes*,[†]

[†]Kavli Nanoscience Institute, Mail Code 114-36, California Institute of Technology, Pasadena, California 91125 and [‡]Electrical Engineering, Case Western Reserve University, Cleveland, Ohio 44106

ABSTRACT We report experimental demonstrations of electrostatically actuated, contact-mode nanoelectromechanical switches based on very thin silicon carbide (SiC) nanowires (NWs). These NWs are lithographically patterned from a 50 nm thick SiC layer heteroepitaxially grown on single-crystal silicon (Si). Several generic designs of in-plane electrostatic SiC NW switches have been realized, with NW widths as small as ~20 nm and lateral switching gaps as narrow as ~10 nm. Very low switch-on voltages are obtained, from a few volts down to ~1 V level. Two-terminal, contact-mode "hot" switching with high on/off ratios ($>10^2$ or 10^3) has been demonstrated repeatedly for many devices. We find enhanced switching performance in bare SiC NWs, with lifetimes exceeding those based on metallized SiC NWs.

KEYWORDS Nanoelectromechanical systems, nanowires, switch, silicon carbide, mechanical computation

Power consumption is a bottleneck for continued and aggressive miniaturization of computing and memory technologies in Si MOSFETs (metal−oxide−semiconductor field-effect transistors), which are currently scaled to the 32 nm technology node (with gate length $L_G \sim 25-30$ nm).[1] However, MOSFET device scaling may soon be limited by the accompanying increased static power consumption.[2] At the device level, it is the increasing leakage that plagues the transistors as they are made ever smaller—because of leakage currents, the device is not truly "off" when it is switched "off". Among several noticeable leakage pathways in a MOSFET, gate tunneling and subthreshold ($V_G < V_T$) drain−source leakage are significant; both arise from the scaling of device dimensions (e.g., aspect ratio) and its induced electrostatic scaling (e.g., of supply voltage V_{DD} and threshold voltage V_T, to maintain constant electric field) and quantum effects.[3,4] Although the introduction of high-κ gate dielectrics[5] has alleviated gate tunneling, the issue of off-state subthreshold (drain−source) leakage current I_{off} remains increasingly acute.[2] Because of its exponential nature, $I_{off} \propto 10^{-V_T/S}$ (where $S = (d(\log I_{DS})/dV_G)^{-1}$ is the inverse subthreshold slope,[6] typically 70−100 mV/decade), a ~80 mV reduction in V_T readily increases I_{off} by 10 times. These issues drive a critical need for new types of switching devices with much steeper subthreshold slopes (smaller S values).

One intuitive approach for realizing minimal subthreshold swing (i.e., steeper slope and ideally smallest S) is to exploit mechanical motion—that is, engineering electrical switching via physical contacts of movable components. This could naturally provide zero off-state leakage, because of the open circuit provided by the air or vacuum gap in the off-state. It is worth noting that, historically, mechanical switches and logic were conceived and explored much earlier than their electronic counterparts and have only been supplanted by electronic computing in the past ~50 years.[7] Advances in micro/nanoelectromechanical devices and systems (MEMS/NEMS) in recent decades suggest the possibility of revisiting mechanical logic.[8] In particular, development in NEMS has clearly demonstrated a number of advantageous characteristics for enabling mechanical circuits,[8−10] including very high operating speeds, ultralow operating power, and device footprints smaller than those of MOSFETs. All these merits make the emerging NEMS attractive for logic switches. In fact, at micrometer scale, mechanical structures have been proposed and explored for hybrid MEMS-MOSFETs that could offer improved switching performance.[11,12] From the nanoscale down to the molecular scale, chemically synthesized structures can also make mechanical switches[13,14] and may engender the possibility of scaling up toward ultra-high-density circuits. SiC is promising for NEMS switches because of this wide-band-gap (~2.4−3.3 eV) material's outstanding electromechanical properties (e.g., elastic modulus $E_Y \approx 430$ GPa, density $\rho \approx 2850$ kg/m^3)[15] and, hence, its promise for switches that are suited for high-temperature, high-radiation, and other harsh-environment applications. In this Letter we develop generic top-down NW switches by employing high-quality SiC material; we demonstrate 50 nm thin SiC NW NEMS switches that provide high switching speeds and low actuation voltages down to $V_{on} \sim 1$ V.

Our devices and their variants are essentially based on a generic NEMS design with lateral (in-plane) motion, as illustrated in Figure 1a. It is a two-terminal switch: the movable body of a doubly clamped NW (with dimensions $L \times w \times t$) is wired to source (S); one of the two complementary gates (G1 or G2) is connected to drain (D), while the other gate can be used to actively pull the switch off the

* To whom correspondence should be addressed, roukes@caltech.edu.
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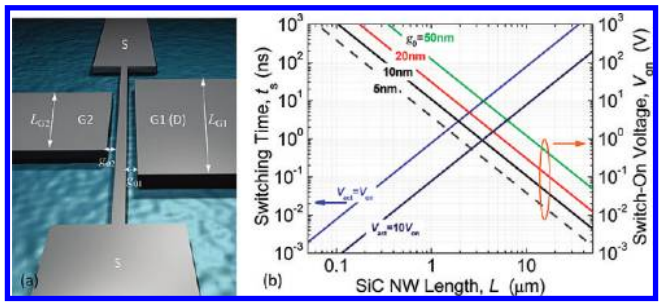

FIGURE 1. NEMS switches based on top-down SiC NWs toward very low voltage and submicrosecond operation. (a) Illustration of a NW switch with complementary lateral gates for actuation and active pull-off. (b) Analytical prediction of the scaling of switch-on voltage (V_{on}) and switching time (t_s) for 50 nm wide, 50 nm thick SiC NWs with length being varied.

contact in case surface forces dominate over the NW's restoring elastic force. The gates' widths and geometries can be altered to explore the effects of varied coupling strength and contact area, as illustrated in Figure 1a. As key specifications of such in-plane mechanical switches, switch-on voltage scales as

$$V_{on} \approx (8k_{eff}g_0^3/27\varepsilon_0 A)^{1/2} \propto \sqrt{E_Y w^3 g_0^3}/L^2$$

and switching time scales as

$$t_s \approx \sqrt{27/2}(V_{on}/\omega_0 V_{act}) \propto (L^2/w)(V_{on}/V_{act})\sqrt{\rho/E_Y}$$

with lumped parameters k_{eff} being the effective stiffness, g_0 the initial coupling gap, A the coupling area, ω_0 the fundamental flexural mode angular frequency, and V_{act} the actual applied voltage, respectively. Note that the scaling relations are also valid for out-of-plane devices, simply by replacing width w with thickness t. Clearly, major challenges include realizing very low V_{on} and very small t_s, as well as optimizing the trade-off between them. It has been commonly understood that $t_s \leq 1$ μs with $V_{on} < 10$ V is very difficult to access in the MEMS domain.[16] As displayed in Figure 1b with the analytical predictions, by moving to nanoscale structures and employing novel NW materials and structures (such as SiC NWs), we can engineer NEMS switches with very low turn-on voltages and submicrosecond switching times. Such low voltage devices could readily find niche applications even if, merely by speed measure, they may still be slower than some of the state-of-the-art MOSFETs.

The SiC layer is made by an atmospheric-pressure chemical vapor deposition (APCVD) heteroepitaxial process which has been optimized for producing high-quality SiC layers (3C-polytype) on single-crystal Si(100), particularly for deep-submicrometer thicknesses and with minimal surface roughness ($R_{q,rms}$),[9,17] which are important prerequisites for enabling top-down NWs. Specifically in this effort, 4-in. wafers of ~45−50 nm thick SiC epilayers with typical $R_{q,rms}$~1.1−2.5 nm are realized for the first time. We have developed two different surface nanomachining processes for making devices. The first (Figure 2a) is a lift-off process: starting from a 50 nm SiC layer on Si, spin-coating poly(methyl methacrylate) (PMMA), high-resolution electron-beam lithography (EBL) defining the NEMS is performed (using Leica/Vistec EBPG 5000+), followed by metallization

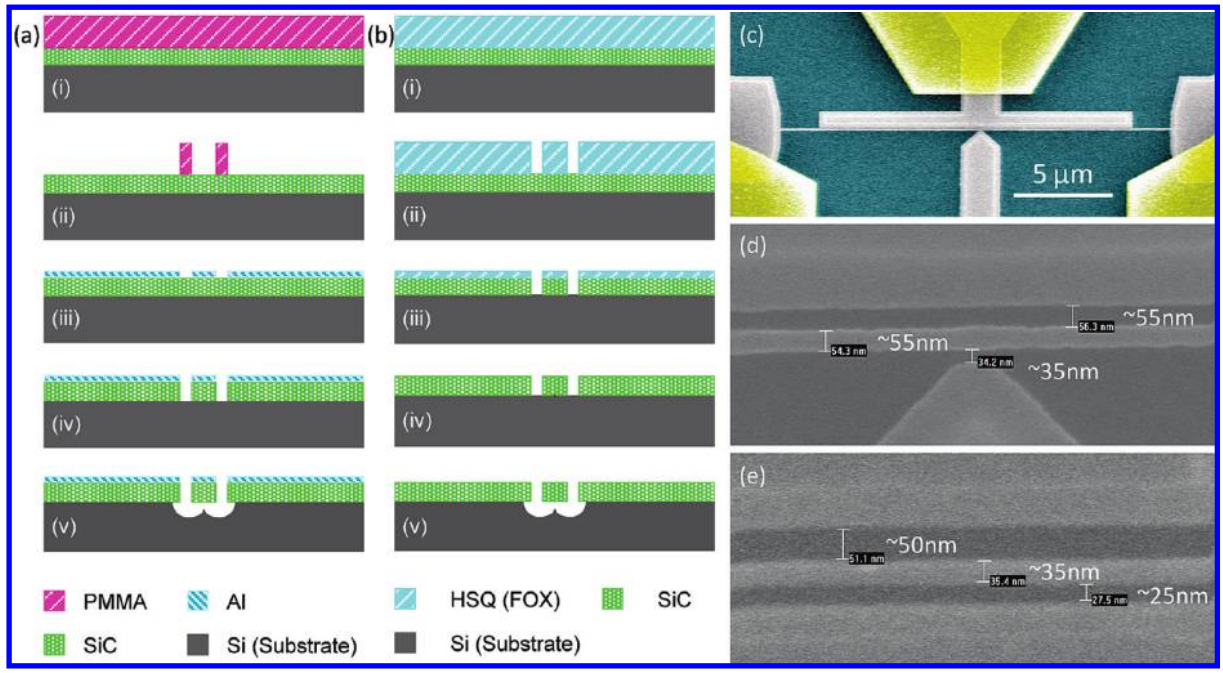

FIGURE 2. Top-down SiC NWs enabled by high-resolution lithography and surface nanomachining. (a, b) Illustrations of the lift-off and negative-mask surface nanomachining processes for making the SiC NWs studied in this work. (c) A 20 μm long SiC NW with a 15 μm wide lateral gate and a point-contact gate. Light gray indicates top Al metallization layer and yellow indicates larger Au pads. (d) Close-in view of the device in (c) showing the thin NW and the gap enabled by the lift-off process. (e) Typical nonmetallized SiC NWs and gaps achieved by the negative-mask process in this work.

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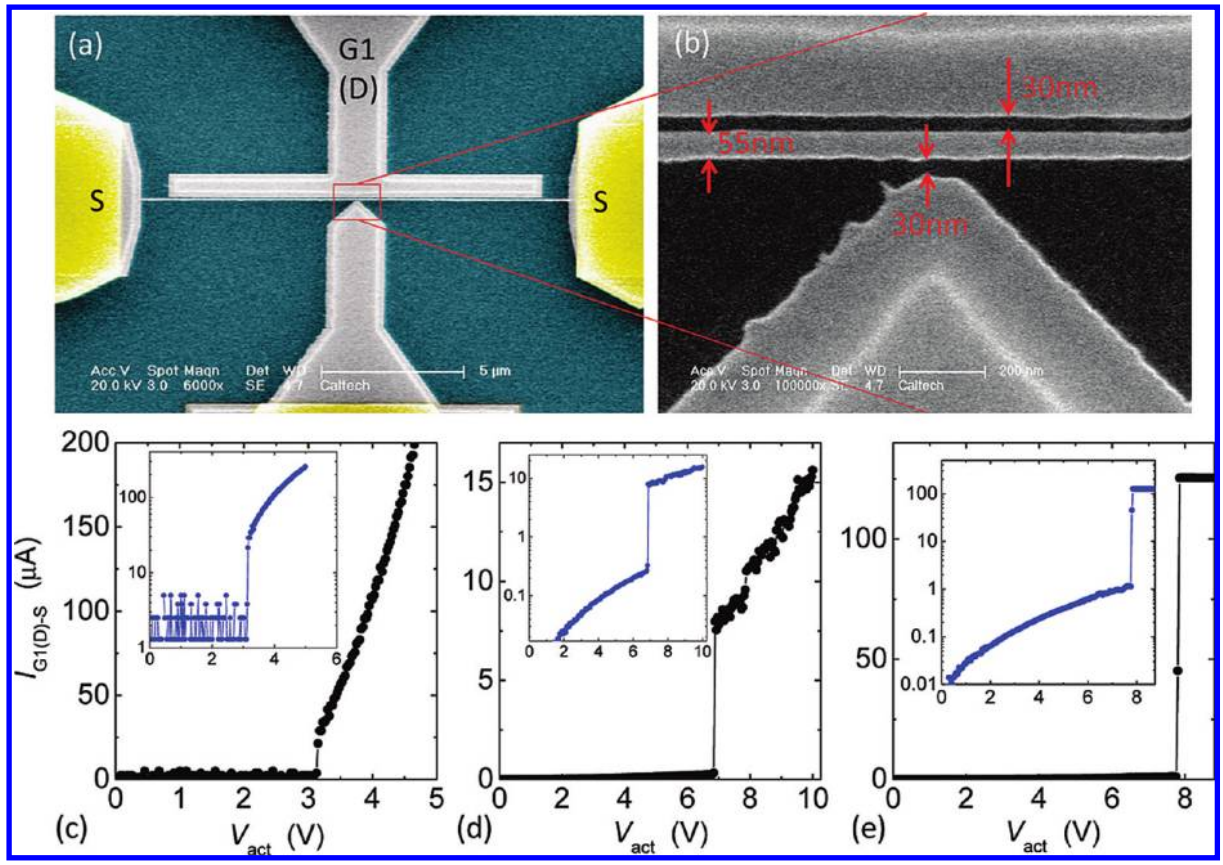

FIGURE 3. Low voltage NEMS switches based on thin *metallized* SiC NWs. (a) A 15 μm long, 55 nm wide SiC NW metallized with 30 nm Al on top. (b) Close-in view showing the 55 nm width and the 30 nm gap enabled by the lift-off process. (c, d) NEMS switching events from two 20 μm long devices, with $V_{on} \approx 3.1$ V and 7.0 V, respectively. (e) Measured switching event from a 15 μm long device, with $V_{on} \approx 7.8$ V. Insets in (c−e) are the data shown with measured current in the logarithmic scale.

with ∼30−40 nm aluminum (Al), and final suspension of devices by a two-step plasma etch (e.g., ECR or ICP) employing the Al metallization as an etch mask (first anisotropic etch of SiC and then an isotropic etch of the sacrificial Si). This process routinely yields metallized SiC NWs with typical widths and lateral coupling gaps of ∼30−100 nm (Figure 2c,d). The second nanomachining process (Figure 2b) uses a negative mask, hydrogen silsesquioxane (HSQ, flowable oxide FOX-12). Here the exposed HSQ remains after EBL (in contrast to PMMA) and serves as the pattern-transferring mask. This process needs no metallization and thus yields bare SiC NWs. Moreover, by carefully controlling the lithography and finely tuning the dry etching (Figure 2b,iii−v), this negative-mask process can yield NWs thinner than 50 nm fairly easily. Indeed, it has enabled some of the thinnest NWs and gaps in our devices (Figure 2e, typical); for instance, with thicknesses and widths of 16−25 nm for a number devices and a minimum 9 nm gap (over a length of $L_{G1} = 6$ μm) measured in one device.

After the devices are electrically assembled and then loaded into a chamber at moderate vacuum (∼1 mTorr), we carefully characterize the devices and measure the two-terminal SiC NW NEMS' switching behavior by using a semiconductor parameter analyzer (HP4145B). We first test the metallized devices made in the lift-off process. For a typical device illustrated in Figure 1a, as we gradually increase the actuation voltage V_{act} between electrodes G1(D) and S, the electrostatic coupling between the gate G1(D) and the movable NW (S) is enhanced. At a threshold voltage $V_{act} \approx V_{on}$, the NW deflects laterally toward the gate to make a contact, and the measured current rises abruptly. Beyond this NEMS switching event, if the contact is Ohmic, the measured current continues to increase linearly as V_{act} is increased further. Several tested SiC NWs with same nominal dimensions as the one shown in Figure 2c ($L \approx 20$ μm, $w \approx 55$ nm, $t \approx 50$ nm, with $t_m \approx 30$ nm Al metallization) have demonstrated similar low switch-on voltage performance. The specific device in Figure 2c and Figure 2d has an initial gap of $g_0 \approx 55$ nm over a 15 μm wide gate (G1). The aspect ratio for the gap is thus $L_{G1}/g_0 \approx 270$, and that for the NW is $L/w \approx 360$. Figure 3c displays the measured $I-V$ characteristics of this particular device, showing a nanomechanical switching event at $V_{on} \approx 3.1$ V. The inset plots the measured current in logarithmic scale. Figure 3d demonstrates the measured data from another device which consists of another 20 μm long NW but a wider coupling gap, $g_0 \approx 90$ nm, showing a switch event at $V_{on} \approx 7.0$ V. We have also achieved very small widths and gaps for 15 μm long

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NWs as shown in Figure 3a. Figure 3b shows one example with NW width $w \approx 55$ nm and a very small gap $g_0 \approx 30$ nm. In this case, the very large aspect ratios are $L/w \approx 270$ and $L_{G1}/g_0 \approx 400$, respectively. Figure 3e shows the measured data from a 15 μm long metalized SiC NW with a measured gap $g_0 \approx 52$ nm, demonstrating an abrupt switch event at $V_{on} \approx 7.8$ V (in this case, upon switch-on, the current rises quickly up to the compliance limit set in the $I-V$ measurement). The low switch-on voltages demonstrated above represent an important merit and improvement enabled by these SiC NW devices. Micrometer-scale beam- or film-structured MEMS switches often require >10 V or sometimes >30−50 V actuation voltages.[18] In fact, in a number of recently reported mechanical switches based on nanoscale structures,[19−21] attaining switch-on voltages substantially lower than 10 V remained very challenging, especially for top-down NEMS switches with controlled patterning and nanofabrication of very thin coupling gaps.

We note that for a few among many of such long NWs with aggressively designed small gaps (sub-50 nm), it has been found that the NWs had stuck to either gate (G1 or G2) after they were suspended by dry etching. Sometimes the gaps realized in lithography and nanomachining are thinner than the designed ones. We have also repeatedly observed, in some devices with very thin gaps (~20 nm or smaller), when we perform high-resolution scanning electron imaging of the devices, the illuminating electron flux and its charging effect can cause the devices to switch on.

In the data shown in Figure 3, we note that in the range of $V_{act} < V_{on}$ (i.e., subthreshold region of these NEMS switches), there are background currents at well measurable levels. These off-state currents are unwanted parasitic leakage. If these are at undesirably high levels, they translate into compromised on/off ratios for the switching devices. On/off ratios of $\sim 10^3$ are clearly not yet ideal and are still far from the fundamental limits for NEMS switches. The parasitic leakage currents we have observed in our measurements are limited either by undesirable instrumental leakage (cable, etc., in the data shown in Figure 3c) or by substrate leakage in the SiC-on-Si material (in the data shown in Figure 3d,e). Fortunately, in this exploration, all of these leakage mechanisms are not fundamental to the generic NEMS switch technology itself. The former issue can be readily eliminated by employing well-calibrated, low-leakage cables and higher-precision instruments. The latter can be resolved by exploiting materials stacks that would provide much better insulation between the thin film device layer and the substrate—such as SiC on insulator (SiO_2) or SiC on Si-on-insulator (i.e., SiC on SOI). Processes based on hydrogen ion (H^+) implantation plus layer splitting, as well as epitaxial growth, have been pursued in recent years.[22−25] We expect that optimizations in such technologies would lead to genuinely nanoscale, high-quality thin SiC films on SiO_2 or on SOI. Once the device-to-substrate insulation is achieved and optimized via proper materials engineering in such new

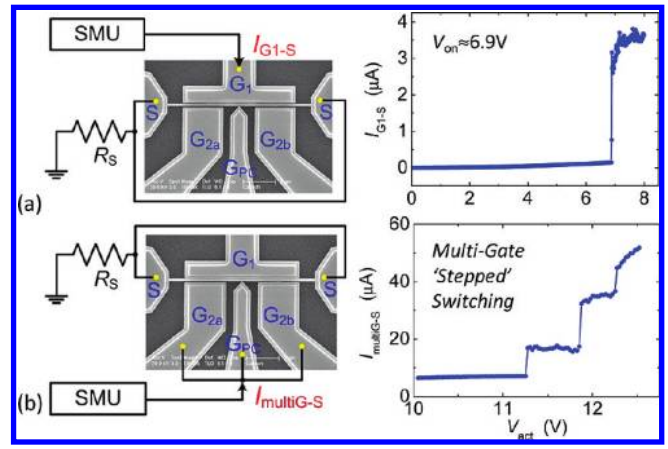

FIGURE 4. NEMS switches based on *metallized* SiC NWs with lateral point-contacts and other complementary gates (SMU = source monitor unit in the HP4145B, R_S is a series resistor that ranges from 40 to 100 kΩ for various devices we have tested). (a) A two-terminal switch showing a $V_{on} \approx 6.9$ V via electrostatic pull-in to the 8 μm wide large gate (G1). (b) Measured two-terminal switching by using the point-contact and the two 3 μm wide gates collectively; the data show a sequential, stepped behavior with the multigates.

wafers, the intrinsic SiC NEMS device leakage would be down to sub-picoampere (10^{-12} A) or even femtoampere (10^{-15} A) levels, along with modern instruments that offer down to ~1 fA level resolution and leakage specifications. This would lead to attaining on/off ratios of $\sim 10^6$ and even higher.

The present top-down SiC NW NEMS have great advantages in permitting flexible, innovative designs and in-plane structural complexity, which remain to be elusive for today's state-of-the-art bottom-up NW NEMS.[26] We have realized metallized SiC NWs with *multiple* lateral gate electrodes, including a point-contact gate (Figure 4), by using the metallization/lift-off process. The multigate device in Figure 4 (dimensions $L \times w \times t \approx 10\ \mu\text{m} \times 100$ nm $\times$ 50 nm, with $t_m \approx 40$ nm Al atop) has measured gaps $g_{01} \approx 65$ nm to the upper wide gate (G1), $g_{02} \approx 80$ nm to the lower gates (G2a and G2b), and $g_{0PC} \approx 35$ nm to the point-contact gate (G_{PC}), respectively. Two-terminal switching by using G1 as the actuation gate demonstrates $V_{on} \approx 6.9$ V (Figure 4a). Alternatively, as we wire the three lower gates together and employ them as one collective actuation gate (Figure 4b), the measured data clearly demonstrate an interesting switching behavior with sequential steps of abruptly increased current, occurring at $V_{act} = 11.3$, 11.9, and 12.3 V. This characteristic of multigate devices is quite interesting and intriguing. It strongly suggests that the interplay between the local coupling strength at each gate and the NW's local rigidity for in-plane deflection may be independently detected and registered; different segments of the NW seem to make contacts to the corresponding gates locally, as the actuation voltage is swept up. We also note that, in fact, these multigate devices (including the ones in Figure 2 and Figure 3) can be multifunctional. Besides switches, they also

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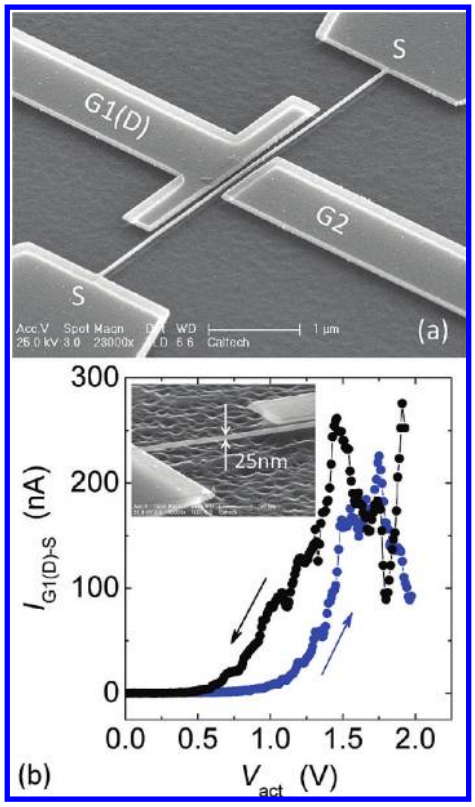

FIGURE 5. Very low actuation voltage NEMS switches based on very thin bare (*nonmetallized*) SiC NWs. (a) Tilted view of a typical device with two complementary gates. (b) A typical measured switching cycle from repeated operations of a 25 nm thin SiC NW, showing $V_{on} \approx 1-1.5$ V and hysteresis behavior. Inset: the close-in view of the suspended device showing the measured 25 nm width.

make very interesting NEMS resonators with integrated electronic or tunneling transduction.[27−29]

In parallel to metallized devices, nonmetallized SiC NWs are also attractive because they allow for straightforward SiC−SiC contacts, instead of metal−metal contacts in a mechanical circuit. Moreover, without metallization, the devices are lighter (leading to higher switching speeds), and our negative-mask process (Figure 2b) readily produces very thin NWs and very small gaps. All of these are favorable motives for pushing toward even lower switch-on voltages and faster switches. Figure 5a shows a typical nonmetallized SiC NW. This specific device has dimensions $L \approx 5\,\mu$m, $w \approx 55$ nm, $t \approx 50$ nm, and $g_0 \approx 60$ nm for coupling gaps to both gates G1 and G2. Furthermore, some bare SiC NWs indeed demonstrate switching behavior at very low actuation voltages. Figure 5b shows measured switching events from an 8 μm long, 25 nm thick SiC NW with a measured switching gap of only 27 nm, showing $V_{on} \sim 1$ V, with clear and repeated hysteretic behavior over many cycles. In contrast to the aforementioned metallized SiC NW devices, which often switched only a few cycles or even just once before fusing (verified by real-time scanning electron imaging), the bare SiC NWs (including the $V_{on} \sim 1$ V one) have performed at least several tens of switching cycles, with no obvious degradation observed. Here the switching-on behavior is gradual and less abrupt compared to that of the metallized devices, presumably because the bare SiC−SiC contacts are much less conductive than the Al−Al contacts, and depend more on the gradual, subtle details of the contact (e.g., evolution of asperities, tunneling, etc., with the increasing contact force) that demand more systematic studies. Later we investigate the failure mode of the nonmetallic devices via high-resolution scanning electron imaging, in real time, while the devices are being switched on and off. In contrast to many metallic devices which fail due to fusing, the nonmetallic devices fail after the NWs deform more and more, and gradually become bent and stuck to the contact electrode. This seems to indicate that the devices have been in stiction or are plastically deformed at failure. The real-time imaging verification of device failure without fusing- or welding-induced damage is important. It is promising to engineer highly conductive SiC nanostructures (also possibly in other tough and high-temperature compatible materials) and innovative surface passivation layers,[30] to achieve $\sim 10^9$ switching cycles in NEMS switches. Table 1 briefly summarizes the specifications and performance of the representative devices discussed in the present work.

In summary, we have developed very thin SiC NWs using two top-down nanofabrication processes and realized several types of new and versatile NEMS devices. Given the very small widths and gaps, these devices make interesting contact-mode nanomechanical switches that offer very low turn-on voltages down to the level of ∼1 V, and also simultaneously offer very short switching times in the submicrosecond range. Such specifications have not been

TABLE 1. Specifications and Performance of Representative SiC NW NEMS Switches

	device 1	device 2	device 3	device 4	device 5
length (μm)	20	20	15	10	8
width (nm)	55	55	55	100	25
thickness (nm)	50	50	50	50	25
metallization on top	30 nm of Al	30 nm of Al	30 nm of Al	40 nm of Al	
switching gaps	$g_0 \approx 55$ nm	$g_0 \approx 90$ nm	$g_0 \approx 52$ nm	$g_{01} \approx 65$ nm ($g_{02} \approx 80$ nm, $g_{0PC} \approx 35$ nm)	$g_0 \approx 27$ nm
switch-on voltage (V)	3.1	7.0	7.8	6.9 (11.3, 11.9, 12.3 sequentially)	1−1.5
switch-on resistance (Ω)	8.7k	409.2k	<62.8k[a]	∼2.0M (∼560k to ∼25k)	∼5−10M
associated data and plots	Figure 3c	Figure 3d	Figure 3e	Figure 4	Figure 5b

[a] Measured current limited by the maximum allowable value preset before the measurement, hence the measurement does not capture the exact switch-on resistance.

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readily accessible previously with conventional MEMS devices. SiC NWs are attractive for making robust and reliable NEMS switches; future engineering of SiC materials and explorations of nanoscale contacts would further advance the performance and reliability of such devices.

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