AN LDMOS VHF CLASS E POWER AMPLIFIER USING A HIGH Q NOVEL VARIABLE INDUCTOR

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Abstract- An LDMOS based VHF Class E power amplifier has been investigated theoretically and experimentally. Simulations were verified by amplifier measurements and a record high class E output power was obtained at 144 MHz in excellent agreement with simulations. The key of the results is the use of efficient device models, simulation tools, and the invention of a novel high-Q inductor for the output series resonance network. The latter allows for low losses in the output network and simultaneously a wide tuning range for maximum output power or maximum efficiency optimization.

I. INTRODUCTION

The Class E amplifier is an attractive solution to obtain a high output power with a high efficiency, the principle of the circuit was first described by Ewing [1] in 1964. Ewing demonstrated an amplifier with 20W output power with 94% efficiency at 500 kHz.

Sokal [2] showed 11 years later an amplifier working in the low MHz range with 26W output power and a drain efficiency of 96%. Closed form equations have been developed by many authors to aid the design of the Class E-amplifier [3]. Due to the evolution of advanced MOS transistor technologies like HEXFET and LDMOS, and the increasing demand of high efficiency amplifiers for mobile communication, the class E concept is again receiving attention and output powers of up to 400 W have been obtained in the HF band [4].

In the VHF-range and higher, some experimental results have been obtained but the output power has so far been limited [5,6]. In this work, a novel concept of the output network and the usage of the newly developed silicon LDMOS device made it possible to achieve a record high output power of 54 W with a comparatively high efficiency of 70% at a frequency of 144 MHz. We believe that the results can be scaled up both in power and frequency.

II. THE CLASS E AMPLIFIER

The switched-mode class E amplifier is ideally based on the characteristic topology according to Fig 1 where a switch is charging a choke with magnetic energy during the 'on'-time of the switch while during the 'off'-time, the energy is released partly to the parallel capacitor Cp and partly to the output network which consists of a load in series with a series resonance circuit.

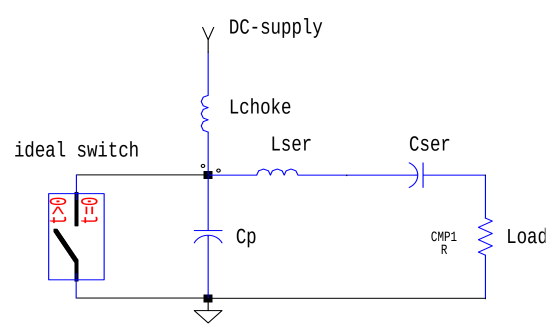

Fig 1 Ideal Class E Amplifier circuit

The switch is in our work realized by an LDMOS-transistor driven by a voltage applied at the gate. At frequencies in the VHF-band and higher, neither the switch nor the passive components can be regarded as ideal and the analytical equations described by different authors can not be used anymore for successful optimization of the circuit. The recent improvements in the modeling of active devices and simulation tools have however made it possible to design such amplifiers with sufficiently good accuracy by computer simulation. The LDMOS transistor used in this study is a MRF 183 from Motorola which is able to deliver an output power of 45W with 33% drain efficiency at 900 MHz. A nonlinear model based on the 'Root' model is available at the Motorolas• web-site and can be easily downloded to the simulator.

In order to obtain a practical class E amplifier topology some modifications to fig 1 have to be made. The goal was to obtain the same power from the transistor compared to when it is working in class AB and to investigate the possibility of achieving a high efficiency simultaneously. The capacitor Cp is partly absorbed by the transistor through its output capacitance which for the particular device is 38 pF. The input impedance according to the datasheet is quite low, 1.1+j 0.93 Ω (at 930 MHz) so a matching network consisting of a ferrite transformer and an series inductor was used at the input. A turn ratio of 4 was used in the simulations. In order to increase the output power to the load, the 50 Ω load impedance was transformed to 1.5 Ω by a parallel capacitance and a series inductance. This series inductance is absorbed in the series resonance circuit. The Q-value of the resonance circuit was choosen to be low, of the order of 5, in order to have resonable bandwidth and low sensistivity of the circuit performance to the series resonator values.

III. SIMULATIONS

The device model was inserted in the simulator and the circuit topology in Fig. 2 was used for the simulation and optimization of the circuit.

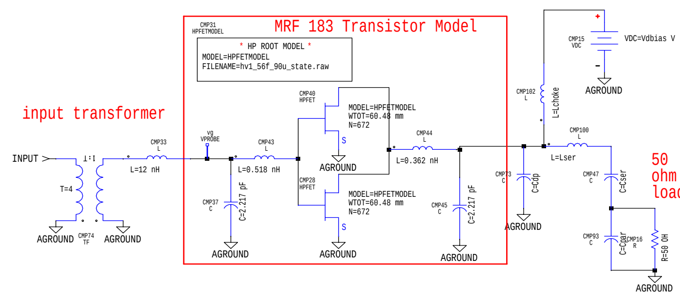

Fig 2 Class E amplifier circuit

The impedance transforming network at the output was determined by a linear simulation, while the choke Lchoke and the capacitor Cdp were optimized for highest efficiency at maximum output power. Lchoke was choosen to have the smallest possible value without sacrifying the efficiency. Component values of the optimized design are listed in Table 1.

Table 1

Cdp	Lch	Lser	Cser	Cpar
55 pF	100 nH	24 nH	120 pF	100 pF

The operation of a class E amplifier is determined by the series resonance network i e the output power and the efficiency is critically dependent on the tuning of this network. The output power, efficiency and different waveforms were therefore investigated a function of the inductance of the series resonance network i e the resonance frequency was swept. Fig 3 shows the output power and Fig 4 the drain- and power added efficiency when this inductor is swept from 10 to 30 nH.

Point b.) refers to maximum power while point a.) and c.) are points off resonance. It is clear from the figures that the highest efficiency is obtained at a higher value of Ls than the value obtained at maximum power i e the resonance circuit should be tuned somewhat lower in frequency compared to the input frequency in order to obtain high efficiency.

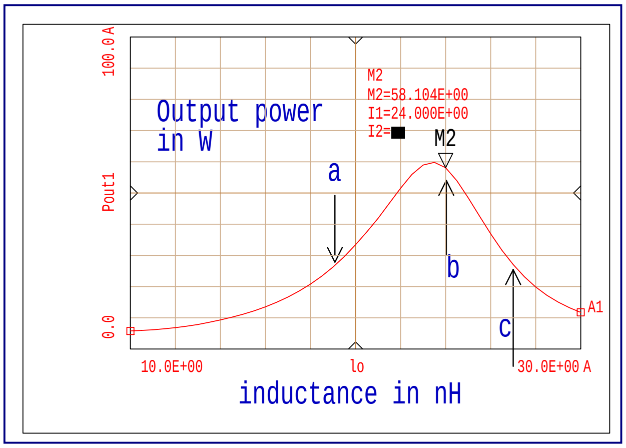

Fig. 3 Output power (in Watt) versus series inductance

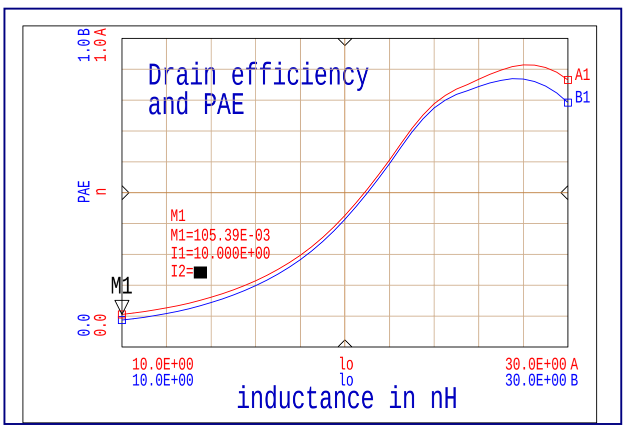

Fig. 4 Drain efficiency and power added efficiency versus series inductance

The predicted maximum drain efficiency is 92% at an output power of 20W. At the maximum power point, 60W, the drain efficiency is 70%. From this simulation it is clear that the output power can be readily tuned by the series resonance inductor.

IV. DESIGN OF THE AMPLIFIER

When all component values were optimized, passive components were selected from the basis of S-parameter characterization. Ld was fabricated by using a tinned wire with a diameter of 0.5 mm, and the input transformer was made by using a binocular type nickel-zinc ferrite of type Fair-rite 28 43 002402. For all capacitors except the Vdd-decoupling capacitors, ATC-100 capacitors were used. All components were tested by a HP 8510 vector-network analyzer (VNA) for verification. Since simulations predicted that the circuits is critically dependent of the output series resonance circuit, special care was taken in the design of this part. A novel inductor was invented, using a copper ribbon 5 mm above the groundplane. By inserting a piece of conductor between the ribbon and the groundplane the inductance can be tuned a least a factor of two. The Q value of the inductor is 150-250, depending on the distance to the groundplane as measured by the VNA at 140 MHz. The transistor was mounted on a heatsink and all components were connected by soldering. After assembling the circuit, the amplifier was connected to the bias supply and measurement equipment. The amplifier worked immediately !

V. EXPERIMENTAL RESULTS

The frequency of the generator was set to 144 MHz and the input and output power was measured with a Bird 4421 power meter, the meter has an accuracy of +/-3%. The input power was set to 5W in order to ensure proper switching of the transistor. The measured power/efficiency behavior is close to the predicted with a maximum power of 54 W and an associated drain efficiency of 70%, and an increasing efficiency when Ls is increased further, at 14 W the drain efficiency is 88%. The power added efficiency is decreasing at low output power levels since the output power is decreased while the input power is constant. Decreasing the input power will in principle increase PAE but this was not done in this work.

One interesting feature with the Class E amplifier is the variation of the output power versus the drain supply voltage. The peak drain voltage is of the order three times the supply voltage as can be seen from the waveform simulations up to a point when the drain-breakdown voltage is reached. The voltage across the load is proportional to the drain-peak voltage which means that the power delivered to the load should be proportional to the drain supply voltage squared. If the transistor is properly switched at different drain supply voltages, the amplifier need not be re-tuned when the supply-voltage is changed. This finding was obtained from simulation and was also verified by experiments, see Fig 5, where the measured output power and drain efficiency is plotted as a function of the drain dc-voltage.

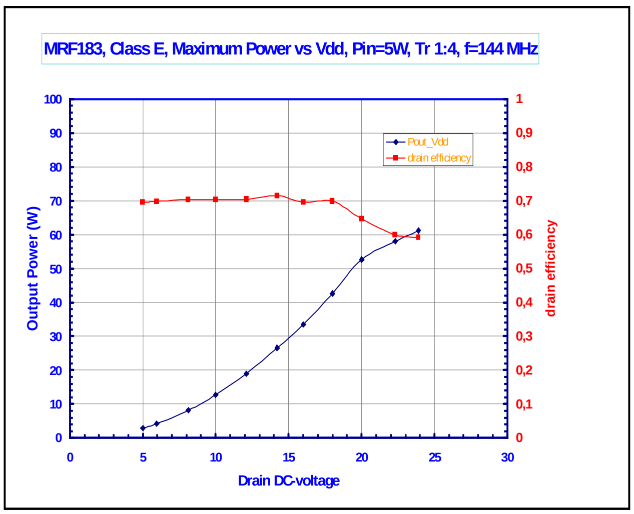

Fig 5 Output power and drain efficiency as a function of the drain supply voltage.

The power vs drain voltage is clearly quadratic up to a point when the drain efficiency start to drop. We believe the deviation above Vdd=18V is due to breakdown in the transistor. The output spectrum was monitored by a HP 8563 Spectrum analyzer. The second harmonic dominated and was typically 38dB below the carrier.

VI. SUMMARY

A Class E amplifier based on LDMOS-transistors working at VHF was demonstrated by simulations and experiments. A record high power was obtained in class E at this frequency, 62 W, from a single device with 121 mm gatewidth. At a lower power, 14W, the drain efficiency was as high as 88%. The key of this result is proper tuning of the series resonator network, computer simulations with good models, and the use of a novel inductor design. A quadratic output power versus drain bias voltage was demonstrated without any retuning and with a maintained high efficiency.

ACKNOWLEDGEMENTS

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