

A 50mm Copper/Polymer Substrate HBT IC Technology for >100GHz MMICs

J.R. Guthrie, D. Mensa, T. Mathew, Q. Lee, S. Krishnan, S. Jaganathan,
S. Ceran, Y. Betser and M.J.W. Rodwell

ECE Dept., University of California, Santa Barbara, CA, USA

Phone:805-893-8044, Fax 805-893-3262, e-mail arlo@vpeak.ece.ucsb.edu

We report HBT integrated circuits fabricated by substrate transfer on 50mm diameter copper/polymer substrates. Layout and packaging of complex ≈ 100 GHz circuits is facilitated by the microstrip wiring environment and the low ground lead inductance it affords. For ICs operating above 100GHz, the process allows radical scaling of the microstrip dielectric thickness without requiring handling of delicate thinned III-V wafers. The process can provide greatly improved heatsinking. Furthermore, full 50mm wafers can be processed incorporating transferred substrate HBTs, devices which have obtained > 500 GHz f_{max} .

Future communications and radar systems will require complex ICs operating significantly above 100GHz. In addition to transistors of greatly increased bandwidth, severe difficulties with interconnects and heatsinking must be addressed. Recently reported MMIC amplifiers operating at 155GHz[1] and 94GHz[2] required substrate thinning to $75\mu m$ and $50\mu m$ respectively, where heatsinking and via inductance are the driving issues. Handling and lapping of such thinned wafers is difficult, and will become more so as frequencies are increased and the wafers thinned accordingly. Delay sensitive circuits demand short interconnects of high wave velocity (low ϵ_r), and hence dense integration. Compounded with the high bias current density required for high speed HBTs, high power densities will arise and effective heatsinking is required.

We present a Copper/polymer substrate HBT IC process. ICs are fabricated on a 50mm diameter substrate. The Cu/polymer substrate provides a microstrip wiring environment with $5\mu m$ dielectric thickness for low via inductance. As circuit operating frequencies increase, the substrate thickness can easily be scaled further. By virtue of the low permittivity ($\epsilon_r \approx 2.7$) dielectric used, the wiring offers $200\mu m/psec$ propagation. Copper thermal vias and the copper substrate provide effective heatsinking. The process includes transferred substrate HBTs, which have earlier obtained > 500 GHz f_{max} [3].

The InAlAs/InGaAs epitaxial layer structure is reported in[4]. Processing is reported in[4,5] up until the electroplating steps. Initial, thin Au and Ni layers are followed by a $30\mu m$ Cu layer, and a final Ni layer. The wafer is bonded to a Si carrier wafer with wax, in a mounting operation very similar to those used in typical wafer back-thinning processes[6]. The InP growth substrate is removed by a selective wet etch. Collector stripes and final interconnections are patterned while the MMIC wafer resides on the Si carrier. At this stage,

the wafer includes NiCr thin film resistors, Si_3N_4 MIM capacitors, and three levels of interconnect metal. The entire MMIC wafer can then be liberated from the Si wafer in a normal demounting operation, or the MMICs could be diced directly. Schematic cross-sections of the wafer at key steps are shown in figure (1). A photo of a fully processed 50mm diameter wafer is shown in (fig.2).

Transistors with $2\mu m$ collector and $1\mu m$ emitter widths show 175GHz f_t and 320GHz f_{max} (fig. 3). 50Ω microstrip lines show less than 1.1dB of loss at 110GHz (fig. 3).

As a demonstration of this technology, a variety of wideband MMICs have been fabricated on the present 50mm wafer. Darlington feedback amplifiers exhibit 9.5dB of gain from 0 to > 50 GHz (fig.4). Current mirror f_t doubler feedback amplifiers with common emitter input stage exhibited 5.3dB of gain from 0 to > 50 GHz(fig.5). Reactively matched differential cascode f_t doubler amplifiers, designed to drive a 10Ω antenna were also tested on wafer in the 50Ω system. These amplifiers exhibited 8dB of gain from 75-80GHz with respect to 50Ω terminations(fig.6), and would have resulted in ≈ 10.5 dB of gain into the 10Ω load.

The Copper/Polymer substrate process is similar to a conventional microstrip process, except that mechanical wafer thinning is replaced by a selective wet chemical etch. The process can provide very high f_{max} HBTs and a wiring and packaging environment suitable for ICs operating above 100GHz. Full 50mm wafers have been demonstrated.

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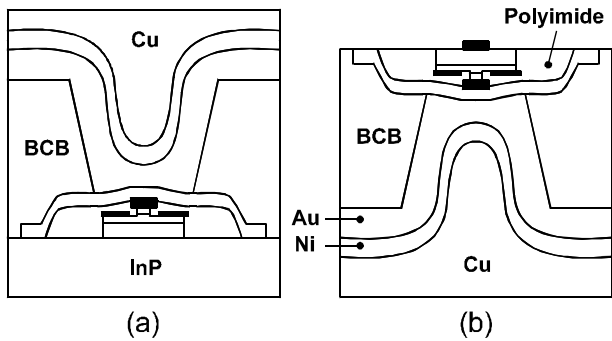
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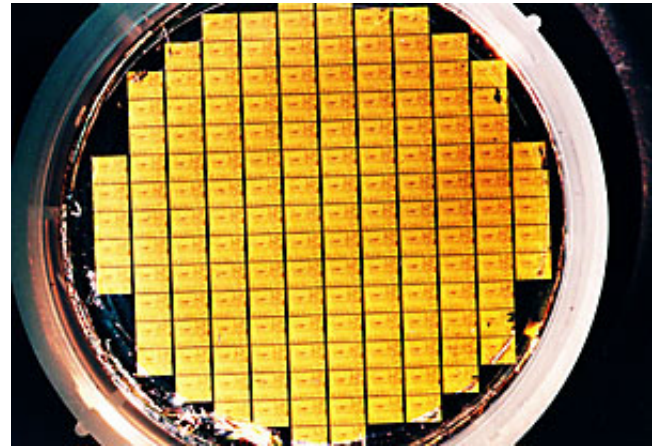
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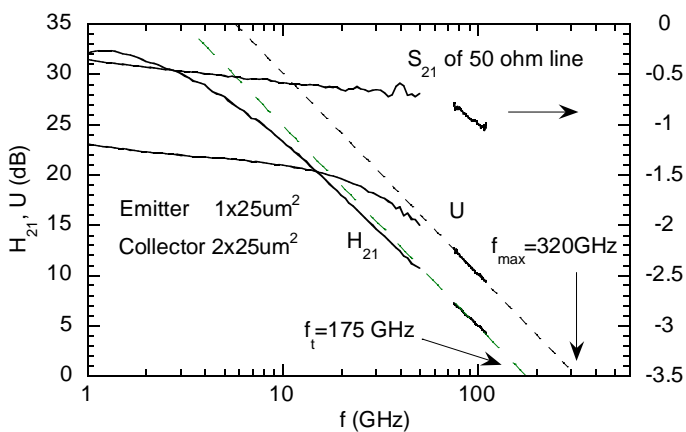
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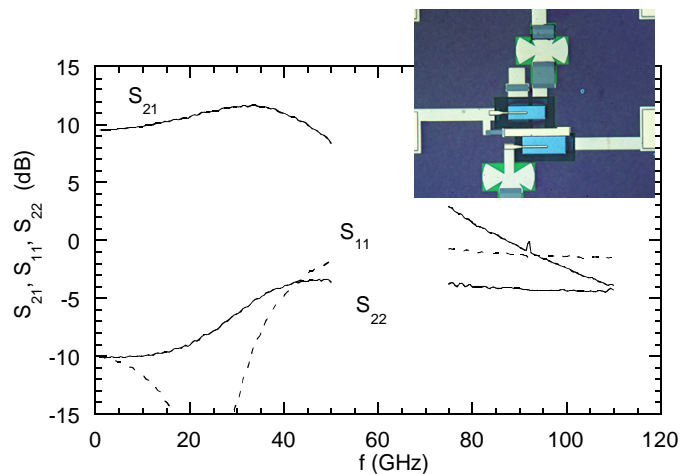
1) Schematic cross-sections at two stages of process: a) immediately prior to InP removal etch b) after InP removal, patterning and deposition of collector contacts.



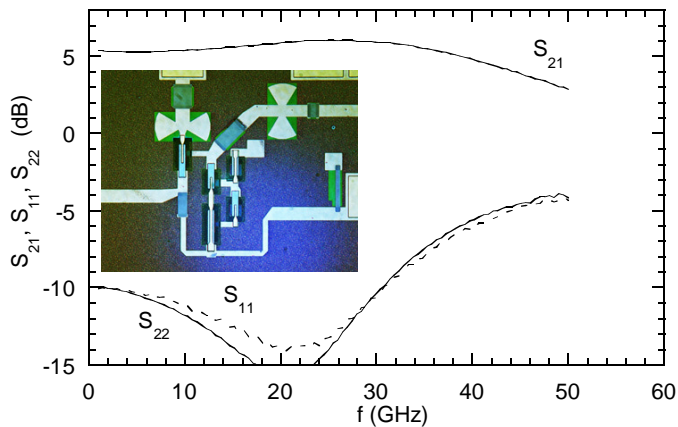
2) Photo of fully processed 50mm diameter wafer.



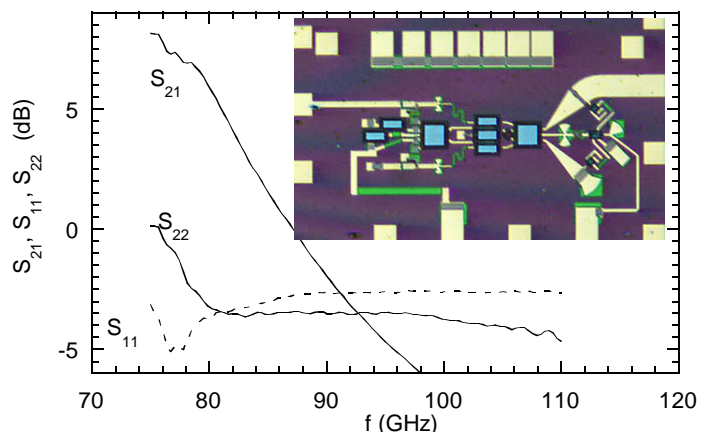
3) Measured RF characteristic gains, H_{21} , U of discrete transistor, and S_{21} of transmission line test structure.



4) Measured RF characteristics of Darlington feedback amplifier. Die photo inset.



5) Measured S parameters of mirror f_t doubler resistive feedback amplifier. Die photo inset.



6) Measured S parameters, with respect to 50 ohm characteristic impedance, of differential cascode tuned amplifier.