Fully Integrated CMOS Power Amplifier Design Using the Distributed Active-Transformer Architecture

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***Abstract*—A novel on-chip impedance matching and power-combining method, the *distributed active transformer* is presented. It combines several low-voltage push–pull amplifiers efficiently with their outputs in series to produce a larger output power while maintaining a 50-Ω match. It also uses virtual ac grounds and magnetic couplings extensively to eliminate the need for any off-chip component, such as tuned bonding wires or external inductors. Furthermore, it desensitizes the operation of the amplifier to the inductance of bonding wires making the design more reproducible. To demonstrate the feasibility of this concept, a 2.4-GHz 2-W 2-V truly fully integrated power amplifier with 50-Ω input and output matching has been fabricated using 0.35-μm CMOS transistors. It achieves a power added efficiency (PAE) of 41% at this power level. It can also produce 450 mW using a 1-V supply. Harmonic suppression is 64 dBc or better. This new topology makes possible a truly fully integrated watt-level gigahertz range low-voltage CMOS power amplifier for the first time.**

***Index Terms*—Circular geometry, CMOS analog integrated circuit, distributed active transformer, double differential, harmonic control, impedance transformation, low voltage, power amplifier, power combining.**

I. Introduction

THE DESIGN of a fully integrated power amplifier with a reasonable output power, efficiency, and gain remains one of the major challenges in today's pursuit of a single-chip integrated transceiver. Although several advances have been made in this direction, a truly fully integrated CMOS power amplifier at watt level output power has not been reported to this date.

Multiple external components such as bonding wires and external baluns have been used as tuned elements to produce output power levels in excess of 1 W using CMOS [1], [2] or Si-Bipolar transistors [3], [4]. Alternative technologies with higher breakdown voltage devices or higher substrate resistivity have been used to increase the output power and efficiency of integrated amplifiers. In particular, LDMOS transistors with a breakdown voltage of 20 V [5] and GaAs monolithic microwave integrated circuits (MMICs) with semi-insulating substrate [6]–[8] have been used to integrate power amplifiers. To date, the highest power levels achieved with fully integrated amplifiers in standard silicon are on the order of 100 mW [9], [10].

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Two main obstacles in the design of a fully integrated CMOS power amplifier are the low drain–gate, drain–source, and drain–substrate breakdown voltages of the transistor and the low resistivity of the substrate. The low breakdown voltage limits the output power and the low substrate resistivity reduces amplifier's power efficiency. These problems are exacerbated as the CMOS transistor's minimum feature size is scaled down for faster operation resulting in lower substrate resistivity and smaller breakdown voltages.

To achieve a larger output power despite the low transistor breakdown voltage, some form of impedance transformation is necessary. This impedance transformation could be achieved using an ideal $1:n$ transformer. Unfortunately, an on-chip spiral $1:n$ transformer on a standard CMOS substrate is very lossy and will degrade the performance of the amplifier greatly [11]–[13]. An on-chip resonant match presents a lower, yet significant, loss [13]. This problem becomes worse as the desired power level increases and/or the transistor breakdown voltage decreases. Another difficulty presented by these methods is the thermal dissipation. By not using any means of power combining, the active device is concentrated in one place, resulting in a higher junction temperature that can lower the long-term reliability or even damage the transistor.

This paper describes a *novel distributed active-transformer power amplifier* (DAT) as an alternative and efficient method of impedance transformation and power combining to achieve a high output power while maintaining an acceptable power efficiency. It overcomes the low breakdown voltage of short-channel MOS transistors and thermal dissipation problems. This new circular geometry can be used to implement linear classes A, AB, and B, as well as the switching mode E/F family [14] of push–pull switching power amplifiers. Details of the passive impedance transformation and power-combining network comparing its efficiency to the conventional methods are presented in a companion paper [13]. Section II explains in more detail the challenges in designing a power amplifier using CMOS technology. In Section III, the design evolution leading to the DAT power amplifier is described. Section IV gives a detailed insight about classes of operations, which might be used with the DAT. Experimental results are presented in Section V.

II. Challenges in Integrated Power Amplifiers

Several problems arise when using submicron CMOS technology without any off-chip components or wire-bond inductors for watt-level fully integrated power amplifiers. Design is-

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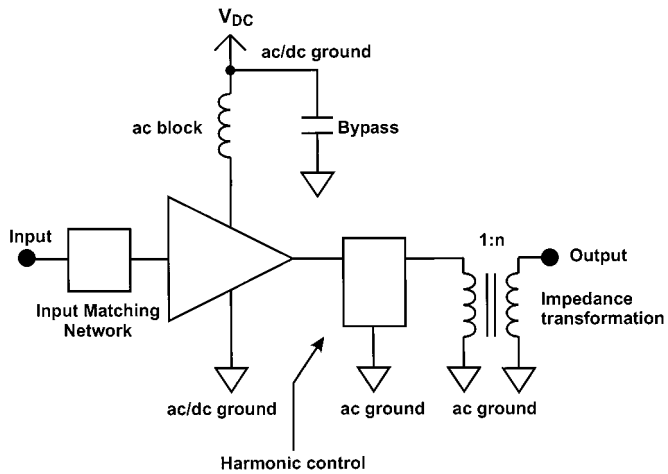

Fig. 1. Block diagram of a power amplifier with critical points for integration.

sues of a power amplifier are described here to illustrate these problems. Fig. 1 shows a simplified diagram of a power amplifier with its key parts.

In terms of frequency response, today's submicron CMOS and/or Si-bipolar technologies offer very acceptable n-channel or n-p-n transistors (e.g., $f_{\max}$ and f_t of 0.15-μm CMOS transistors reach up to 80 GHz). If the only limitation is transistor's speed and gain, in principle it is possible to design switching or linear-mode amplifiers up to the 20 GHz range. Unfortunately, low breakdown voltages and high knee voltages,[1] V_k, of the transistors limit the maximum voltage swing at their drains or collectors. This voltage swing limitations make a large impedance transformation necessary in order to deliver any power beyond 100 mW to 50-Ω loads, R_L. This can be seen from the following calculations for a knee voltage of 0.5 V and supply voltage of 3 V:

$$P_{\text{out}} = \frac{(V_{dd} - V_k)^2}{2R_L} = \frac{(2.5\text{V})^2}{2 \cdot 50\,\Omega} = 63\,\text{mW}. \qquad (1)$$

Another issue is the drain impedance control at the fundamental frequency and at the harmonic frequencies taking into account the transistor parasitic capacitances. Impedance control is required to achieve the desired harmonic suppressions at the output and to improve the drain wave shaping for better power efficiency [15]. This harmonic control must incorporate an inductor, in order to achieve a high-frequency selectivity and to resonate the transistor drain capacitance, as may be seen in the block diagram of the hypothetical power amplifier shown in Fig. 1. Even in class-A operation, in order to satisfy the rigid wireless communications standards, it is necessary to have some harmonic suppression to offset the transistor nonlinearity presented when the power amplifier is operating near its gain compression point.

Due to the series metal resistance and induced currents in substrate, the on-chip harmonic rejection inductor presents a very low quality factor Q. Therefore, this loss component can have a significant effect on the power efficiency of a watt-level submicron CMOS power amplifier in multigigahertz range, typically losing 20%–40% of the power supplied from dc supply in this inductor alone. In order to minimize its loss, the impedance of this inductor should be comparable to the low impedance of the load presented to the transistor and the output impedance of the transistor. For example, to achieve 1-W power with a 3-V supply and a V_k of 0.5 V, the maximum load resistance presented to the transistor may be calculated as

$$R_{l,\max} = \frac{(V_{dd} - V_k)^2}{2P_{\text{out}}} = \frac{(2.5\text{ V})^2}{2 \cdot 1\text{ W}} = 3.1\,\Omega. \qquad (2)$$

Another difficulty brought by this low-impedance inductor is its layout dimensions. For a single-ended amplifier topology, the transistor size has to be large in order to have an acceptable maximum drain current and a low V_k. In this scenario, the physical size of this inductor becomes comparable to that of the transistor making it difficult to establish a low parasitic the connection between the two.

It is also necessary to provide the dc power supply to the amplifier. As shown in Fig. 1, very low-impedance and low-loss connections are required for both ground and positive supply nodes and a high impedance inductor may be necessary to block the ac signal from the power supply. If implemented on-chip, this inductor will have a significant power loss mainly due to the metal resistance. When tuning precision is not required, the dc may be provided by wire bonds. Providing a low-loss and low-impedance ac ground is also a challenge because, unlike in GaAs technology, the silicon substrate is thick and does not have a backside ground plane with via access.

In order to obtain watt-level output power despite the low breakdown voltage of the available devices, one can resort to impedance transformation, power combining, or an amalgamation of both. It is necessary to present to the transistor drain or collector a low impedance, which must be matched to the 50-Ω load. The impedance transformation could be achieved using an ideal $1:n$ transformer. Unfortunately, an on-chip spiral $1:n$ transformer on a standard CMOS substrate is very lossy and will degrade the performance of the amplifier significantly [11]–[13]. Another way to perform the impedance transformation is through a resonant match. A capacitor C_p is connected in parallel to the 50-Ω load R_{load} and an inductor L_s in series, as shown by Fig. 2(a). This transformation can be seen graphically on the Smith Chart of Fig. 2(b). Although this method achieves lower loss than the transformer, its loss is still significant and presents a layout problem similar to that described previously for the impedance control inductor [13].

In the input network of Fig. 1, it is necessary to place an inductor in parallel to the gate to resonate the gate capacitance in order to match the low gate impedance to 50-Ω input. Besides the loss associated with this component and the difficulty in obtaining the necessary low-impedance low-loss ground, the input network also necessitates a low impedance dc block for gate biasing. Although easily implemented by an on-chip capacitor,

[1]Knee voltage is defined to be the voltage below which the device ceases to operate as a transconductance. For the MOS device, it is the voltage below which the device operates in the triode region [15].

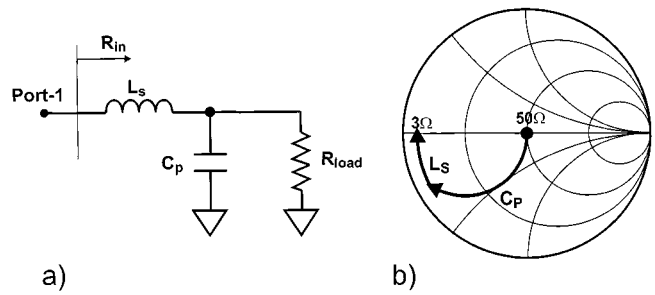

Fig. 2. (a) Resonant impedance transformation network. (b) Its impedance transformation shown graphically using a Smith chart.

the large size of this dc block is undesirable since it consumes a large die area.

III. Distributed Active Transformer

As described in the previous section, there are many challenges in designing a watt-level power amplifier in CMOS. The *distributed active transformer* (DAT) addresses these problems reducing their effects significantly, thus allowing the design of a truly fully integrated power amplifier realizable using submicron CMOS technology.

The DAT combines several low-voltage push–pull amplifiers efficiently to produce a larger output power while maintaining a 50-Ω match. It also uses virtual ac grounds and magnetic couplings extensively to eliminate the need for any off-chip component such as inductors, capacitors, and tuned wire-bond inductors. Furthermore, it desensitizes the operation of the amplifier to the inductance of bonding wires and makes the design more reproducible.

This section describes the design evolution leading to the distributed active-transformer power amplifier. It is worthwhile to note that although the approach is described for MOSFETs here, this architecture may be implemented in a similar way using other technologies such as bipolar junction transistors, metal-semiconductor field effect transistors (MESFETs), or high electron mobility transistors (HEMTs).

A. Differential Push–Pull Topology

The basic building block of the new topology is the push–pull amplifier shown in Fig. 3. This topology creates a virtual ac ground at the power supply and ground. Because these virtual ac grounds are created by symmetry, they are inherently low loss and low impedance. They also avoid the need for a lossy on-chip choke inductor. The connection from these ac virtual grounds to the positive supply and ground will carry only current at dc and even harmonics, thus eliminating the loss caused by the RF signal at the fundamental frequency and odd harmonics going through lossy supply lines. Furthermore, this effect desensitizes the operation of the amplifier to the inductances of bonding wires, making the design more reproducible. It also eliminates the need for a large on-chip bypass capacitor on the supply.

Fig. 4(a) and (b) shows a push–pull amplifier illustrating the impedances seen by even and odd harmonics, respectively. The

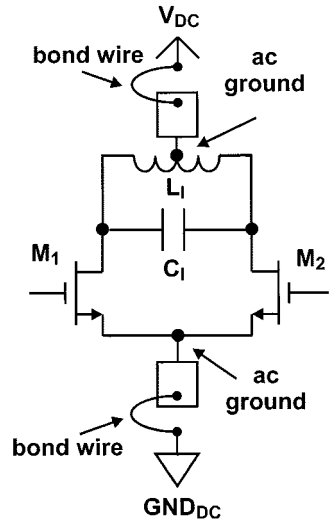

Fig. 3. Push–pull amplifier with virtual ac grounds at the power supply and ground.

differential output signal, $V_1 - V_2$, does not contain any even harmonic components due to symmetry, as demonstrated by the following equations.

$$V_1 = A_1 \cdot \cos(\omega t + \theta_1) + A_2 \cdot \cos(2\omega t + \theta_2) + A_3 \cdot \cos(3\omega t + \theta_3) + \cdots \quad (3)$$

$$\begin{aligned} V_2 &= A_1 \cdot \cos(\omega t + \theta_1 + \pi) + A_2 \cdot \cos(2\omega t + \theta_2 + 2\pi) + A_3 \cdot \cos(3\omega t + \theta_3 + 3\pi) + \cdots \\ &= -A_1 \cdot \cos(\omega t + \theta_1) + A_2 \cdot \cos(2\omega t + \theta_2) - A_3 \cdot \cos(3\omega t + \theta_3) + \cdots \end{aligned} \quad (4)$$

$$V_1 - V_2 = 2A_1 \cdot \cos(\omega t + \theta_1) + 2A_3 \cdot \cos(3\omega t + \theta_3) + 2A_5 \cdot \cos(5\omega t + \theta_5) + \cdots \quad (5)$$

where A_n and θ_n are the magnitude and phase of the nth harmonic at the drain of transistor 1, and ω is the fundamental angular frequency. The elimination of the even harmonics, especially the second, by the circuit symmetry allows for the use of a lower loaded Q—and therefore lower loss—resonant circuit at the drain for harmonic suppression as it only needs to suppress odd harmonics.

If switching modes of operation are desirable, the differential symmetry of this topology provides high impedances, $\sim 2Z_{Vdd}$, at each even harmonic to the transistor drains regardless of the impedances of the output resonant network, Z_l, at these frequencies, as shown by Fig. 4(a). The transistor drain impedances at odd harmonics will be Z_l, as can be seen in Fig. 4(b) and the following equations.

$$\begin{aligned} Z_{\text{even}} &= \frac{V_1}{I_1} = \frac{I_1 \cdot Z_l + (I_1 + I_2) \cdot Z_{vdd}}{I_1} \\ &= \frac{I_1 \cdot Z_l + 2I_1 \cdot Z_{vdd}}{I_1} = Z_l + 2Z_{vdd} \approx 2Z_{vdd} \end{aligned} \quad (6a)$$

$$\begin{aligned} Z_{\text{odd}} &= \frac{V_1}{I_1} = \frac{I_1 \cdot Z_l + (I_1 - I_2) \cdot Z_{vdd}}{I_1} \\ &= \frac{I_1 \cdot Z_l}{I_1} = Z_l. \end{aligned} \quad (6b)$$

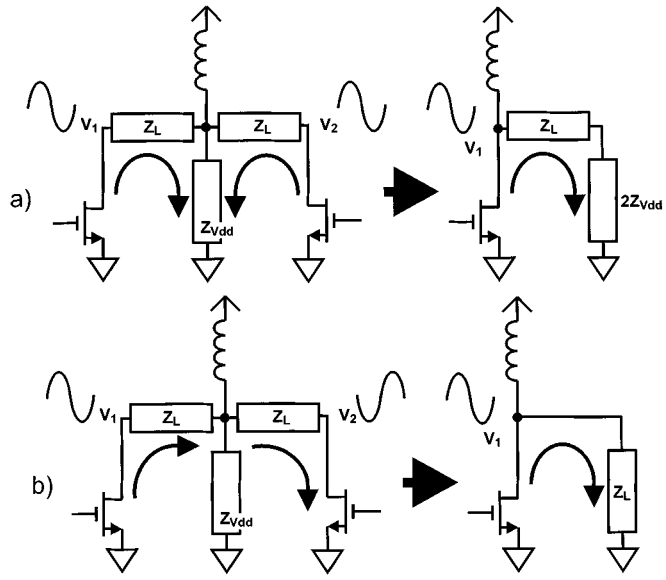

Fig. 4. Effective impedance at the transistor drain. (a) Even harmonic signals. (b) Odd harmonic signals.

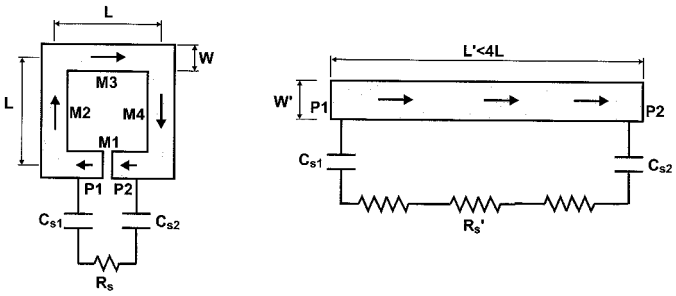

Fig. 5. Comparison of the loss mechanisms for a one-turn spiral and a slab inductor.

By providing a short circuit between the drains at each odd harmonic using a simple parallel *LC* tank tuned to a frequency slightly above the fundamental frequency, the drain impedance will be inductive at the fundamental and will be small at odd harmonics and large at even harmonics. If transistors are driven into saturation, these impedances shape the drain waveforms to perform the high efficiency class E/F_{odd} operation [14].

B. Slab Inductor

On-chip slab inductors[2] present a significantly higher Q and consequently lower loss when compared to conventional low-impedance single-turn spiral inductors. Several factors contribute to the higher Q of the slab inductors. First, the negative mutual inductance between the current through metals on the opposite side of the spiral are reduced. Hence, the total metal length to obtain the same inductance is shorter than the circumference of the loop. Therefore, the resultant inductor demonstrates a lower total series metal resistance, as shown in Fig. 5. Second, the shunt resistance through the substrate between the two terminals of the inductor, P_1 and P_2, will be higher because of the larger distance between them, as illustrated in Fig. 5. Thus, the substrate current and power loss caused by it will be reduced. Third, the metal width of the inductor may be increased beyond the maximum set by the spiral geometry. With wider metal, the series metal resistance is reduced, although capacitive coupling to the substrate is increased. This allows a better optimization of the inductor and in many cases the total loss can be significantly reduced.

[2]Slab inductors are two-port inductors formed by a straight piece of metal, as opposed to curled metal used in one- or two-port spiral inductors.

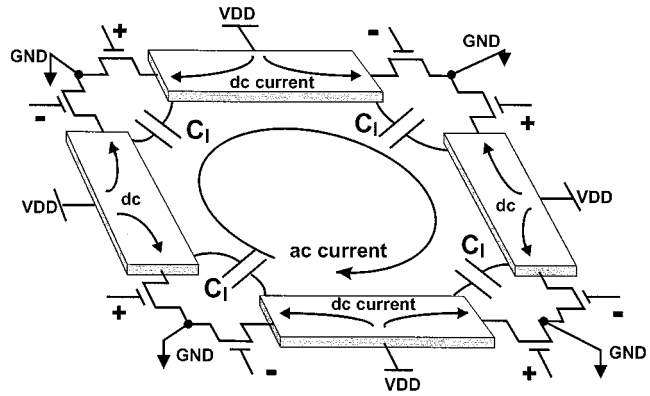

Fig. 6. Circular geometry power amplifier with four push–pull amplifiers and eight transistors.

A slab inductor is used as drain inductor L_l, as shown in Fig. 3, in order to control the impedances at the fundamental frequency and harmonics and also to provide a path for the dc supply current.

C. Circular Geometry

Circular geometry is a means to create low-loss low-impedance virtual ac grounds while using several power amplifier blocks simultaneously. For instance, Fig. 6 shows the primary circuits with four push–pull power amplifiers and eight transistors.

This architecture allows the creation of virtual ac grounds without having to connect together the sources of the pair of transistors of each push–pull amplifier, as shown in Fig. 3. With slab inductors, this connection is physically impossible, without compromising the amplifier operation, as the slab inductors create a large distance between the sources. If a long metal line is used to connect the sources of this pair of transistors, the inductance of this metal will be comparable to that of the drain slab inductor. The resulting source degeneration inductor will seriously degrade the amplifier performance and hence should be avoided.

AC virtual grounds for the fundamental and all odd harmonics can be created in the corner points of the circular geometry by connecting together the sources of the transistors of the adjacent push–pull amplifiers. By driving these transistors in opposite phase, as shown in Fig. 4, their source currents, which belong to different push–pull amplifiers, have the same amplitude and the opposite phase and therefore cancel each other. The result is similar to connecting the sources of the pair of transistors belonging to the each push–pull amplifier with short low-impedance connection. Two electrical diagrams show how four push–pull amplifiers of Fig. 7 are rearranged to form the circular geometry of Fig. 8.

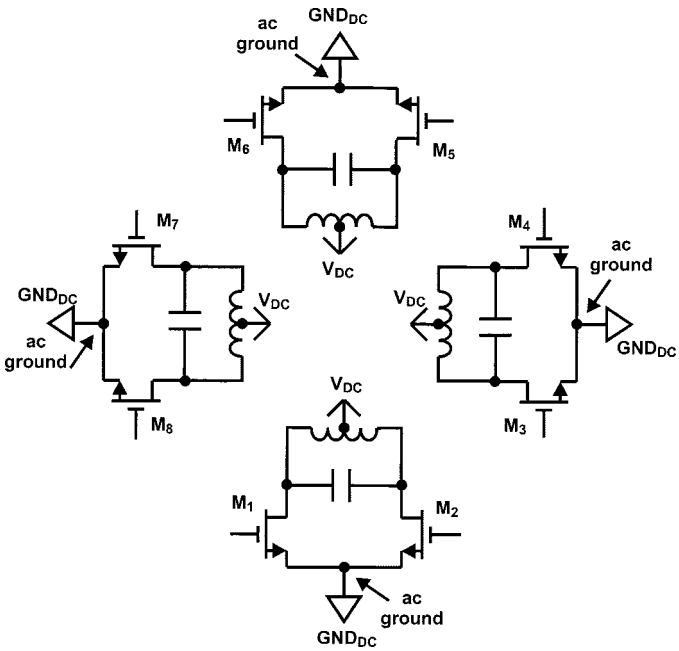

Fig. 7. Four conventional push–pull amplifiers using virtual ac grounds.

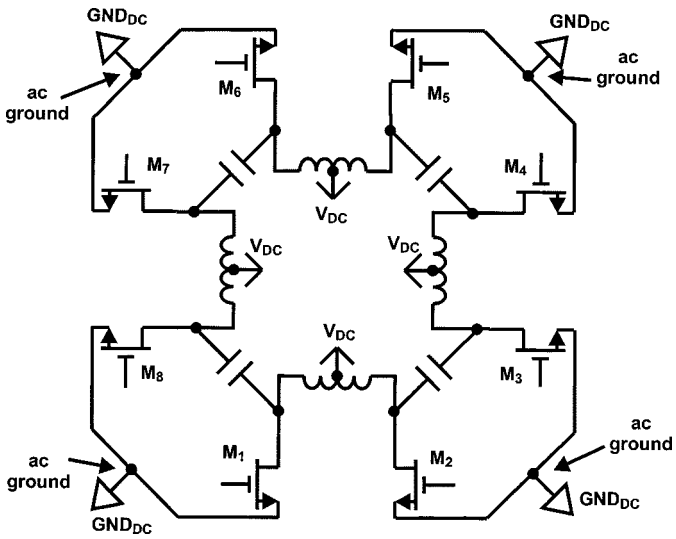

Fig. 8. Four push–pull amplifiers connected in circular geometry creating ac grounds between the adjacent push–pull blocks.

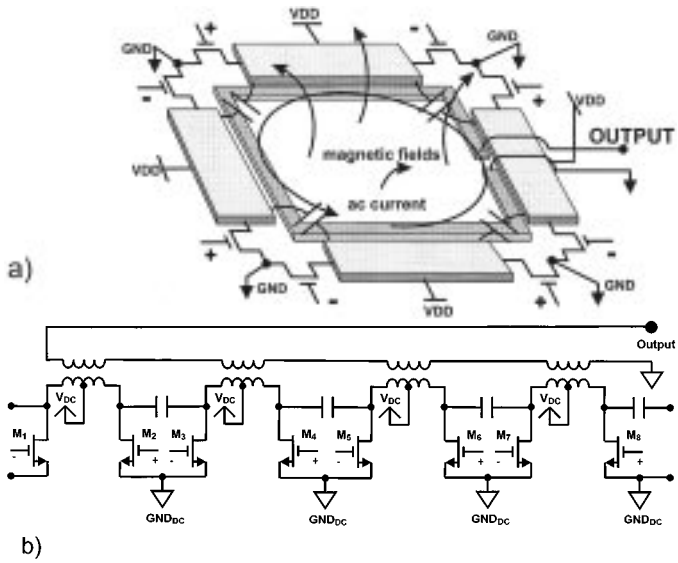

Fig. 9. (a) Distributed active-transformer amplifier with four push–pull blocks and eight transistors. (b) Its corresponding electrical diagram.

D. Cross-Connected Capacitors

The connection of the drain tank capacitor presents similar difficulties. These capacitors cannot be connected between the drains of transistors belonging to the same push–pull amplifier in a conventional way, as the inductance of the long metal lines used to connect them will be comparable to that of the drain slab inductor. In order to solve this layout problem, these capacitors are connected between the drains of adjacent transistors of the circular geometry belonging to the adjacent push–pull amplifiers, as seen in Fig. 6. The voltage between the drains of these adjacent transistors is identical to the voltages between the drains of a single push–pull amplifier, so long as the transistors are driven in proper phase, as shown in Fig. 6. Therefore, if we connect the capacitors between the drains of adjacent transistors, their currents remain exactly the same and the circuit operation does not change. This produces a harmonic suppression and wave shaping identical to connecting the capacitor across the drains of each differential pair.

E. Distributed Active Transformer Power Combining

Although the circular geometry introduced in Section III-C allows several push–pull amplifiers to be designed to reduce the serious layout and thermal dissipation problems, their output powers must still be combined and delivered to the load.

This power combining is accomplished by introducing a one-turn metal strip inside the circular geometry to act as a magnetic pickup of the output power, as shown in Fig. 9(a). The $n/2$ push–pull amplifiers (four in this example), conduct identical synchronized ac currents at the fundamental, inducing corresponding ac magnetic fields in this secondary loop. The internal metal loop harnesses the induced magnetic field to generate a voltage between its terminals equivalent to the sum of the differential voltages of the $n/2$ push–pull amplifiers. Another way to interpret this is to view this topology as $n/2$ push–pull amplifiers each with a $1:1$ transformer, whose secondary circuits are connected in series. As the primary circuits of these transformers are independent, the result is a $1:n$ impedance transformation as in Fig. 9(b). This *distributed active transformer* (DAT) architecture results in a *simultaneous* $1:n$ *impedance transformation and* n *transistor power combining*.

This DAT architecture is completed by proper tuning of the cross-connected drain capacitors and the introduction of a capacitor in parallel with the load. Both are necessary to partially compensate the leakage inductances created by the relatively low coupling coefficient (e.g., $k \approx 0.6$) of the transformer.

F. Cross-Connected Gate Matching

Inductors should be placed in parallel with the transistor gates to resonate the gate capacitance as the input impedance of any transistor large enough to obtain watt-level output power is much lower than that of the 50-Ω input.

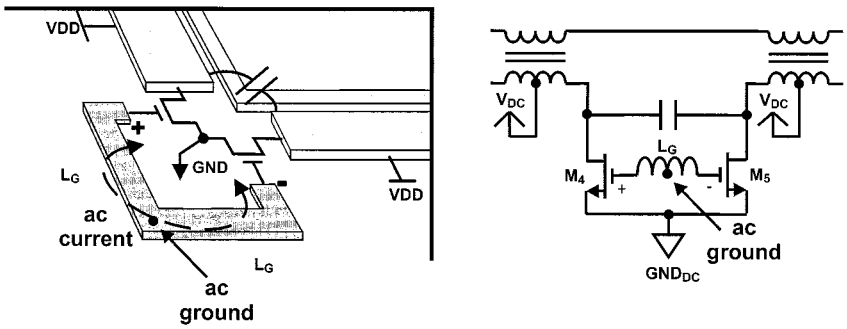

Fig. 10. Cross-connected gate matching inductor.

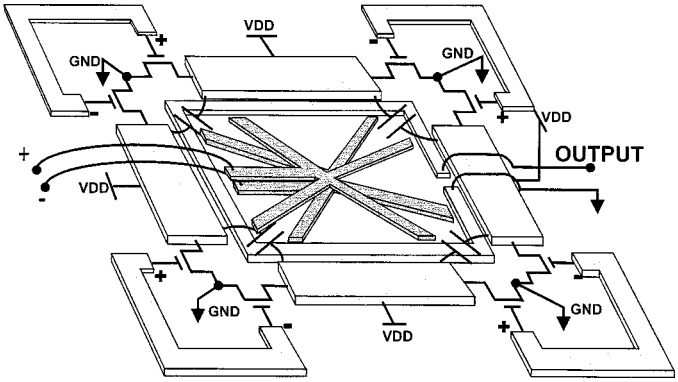

Fig. 11. Input power distribution network.

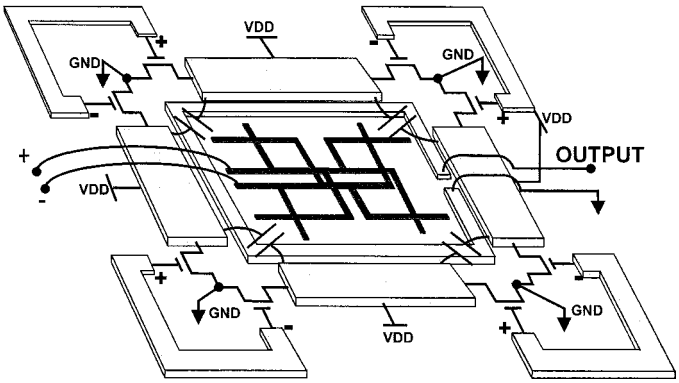

Fig. 12. Input power distribution network with twisted layout to provide a magnetic positive feedback from the output.

This inductor can cause difficulty as there is no convenient ac ground to which to connect it, and its connection to circuit (dc) ground will necessitate an undesirable bypass capacitor. If the gate matching inductors of the adjacent transistors are connected to each other instead of circuit ground as shown in Fig. 10, an ac ground at the fundamental frequency is formed at this connection point and no connection to dc ground is formed, avoiding both problems. Since this connection point can be located far from the transistors, slab inductors can be used to reduce the loss in this component.

G. Input Power Distribution

The power distribution network shown in Fig. 11 brings the synchronized differential power to the gates of the transistors. It consists of two parts, namely the connecting differential lines bringing the balanced signal to the center of the circular geometry, and a distribution network symmetrically connecting the center point to the gates of each transistor.

The differential input can be generated either by an on-chip balun matched to the unbalanced 50-Ω input or by an integrated differential pre-amp stage.

These input power-distributing lines may have a twisted layout, as in Fig. 12, to introduce an adjustable amount of magnetic positive feedback to enhance the gain.

IV. Modes of Operation in Distributed Active Transformer Power Amplifiers

The harmonic impedances available at drains in the distributed active transformer described in Section III-A allow the DAT to operate in several different classes including A, AB, B, C, E, inverse F [16], [17], and E/F_{odd}. A DAT power amplifier can operate in one or more classes of operation depending on the gate bias level, drive level, and drain tuning.

In this section, we analyze the DAT power amplifier starting in either class A or class B and compressing to class E/F_{odd}. These two combinations are the most useful ones when the transistor gain is limited, as class A and B biasing conditions extract the highest gain from the transistor. Starting in class A results in a higher gain, while class-B operation results in a higher drain efficiency. If the operating frequency is low relative to transistor speed and very high transistor gain is available, other choices might be useful.

In the following subsection, we will investigate the DAT operation in classes A, B, and E/F_{odd}. To simplify and clarify the analysis, the push–pull block is further divided into three sub-blocks, namely the input network, the active devices, and the output network. The input network comprises every passive component from 50-Ω input to transistor gates, the active devices block consists of transistors and gate matching inductors, and the output network is formed by the passive components from the drain to the 50-Ω load including the transformer and matching capacitors, as illustrated in Fig. 13.

A. Class A Operation

A straightforward analysis may be performed to calculate the gain, the maximum output power, and the power efficiency as a function of the active and passive parameters and the supply and bias voltages. We assume that the transistor is a linear current source with a transconductance g_m. We assume perfect linearity

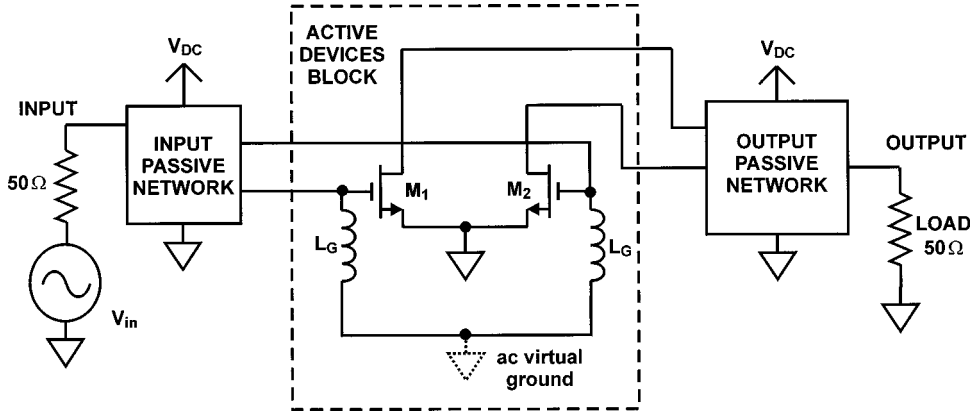

Fig. 13. Three building blocks of a DAT: input network, active device, and output network.

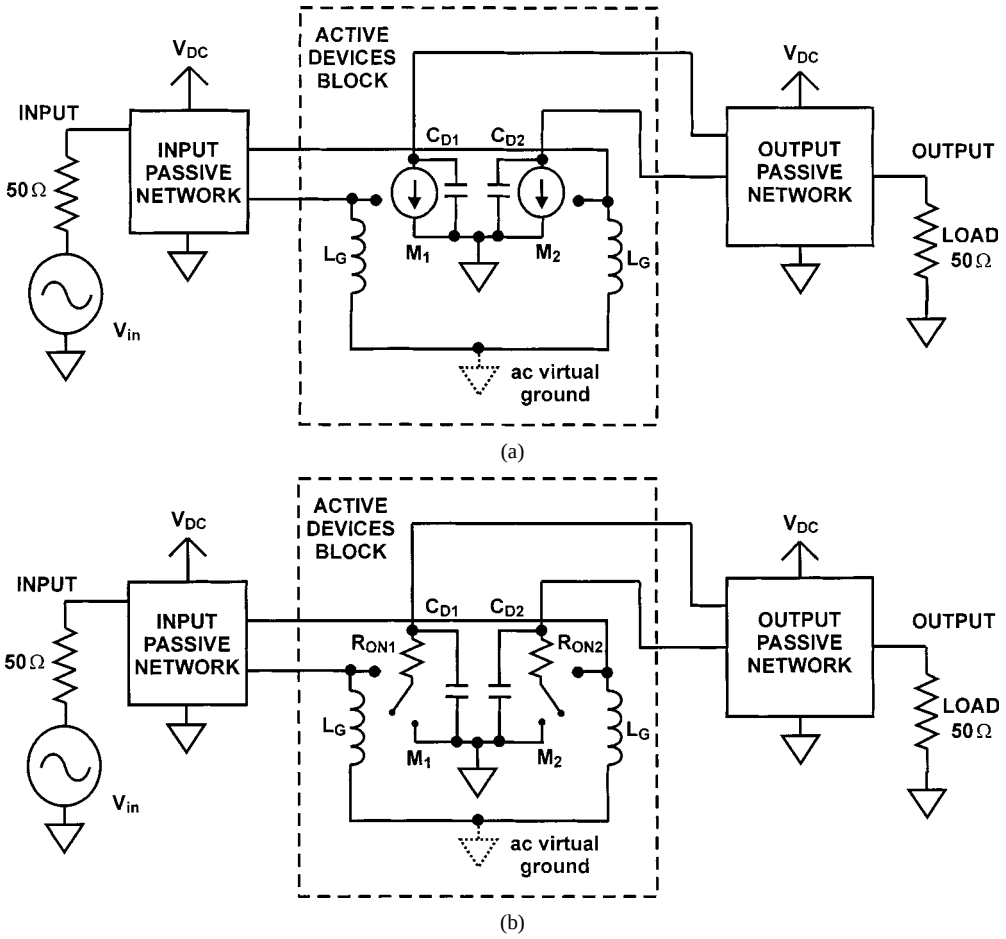

Fig. 14. (a) DAT operating in class A or B mode. (b) DAT operating in class E/F_{odd} mode.

in this case. An equivalent electrical diagram of a push–pull block operating in class-A mode can be seen in Fig. 14(a).

The maximum output power P_{out} will be a function of the transistor knee voltage V_k, [15], supply voltage, V_{dd}, number of combined push–pull blocks, $n/2$, output passive network power efficiency, η_{out}, and load resistance seen by each drain, R_l, i.e.

$$P_{\text{out}} = n \cdot \frac{(V_{dd} - V_k)^2}{2R_l} \cdot \eta_{\text{out}} \tag{7}$$

where R_l is the real impedance seen by the drain of each transistor in the output network, which includes the effect of the output network losses and the load resistance. This value can be calculated using an electromagnetic simulator or approximated analytically [13]. The output capacitance of each transistor is resonated out by the tuning inductance of the output passive network, so that the load impedance including this capacitor is purely real.

The gain will be the product of the active device gain G_A and the input and output passive network power transfer efficiencies η_{in} and η_{out}, i.e.

$$G = \eta_{\text{in}} \cdot G_A \cdot \eta_{\text{out}}. \tag{8}$$

The active device gain G_A may be calculated as a function of transistor transconductance g_m, the gate voltage V_g, the gate matching inductor and transistor equivalent parallel input resistance R_g, and drain load differential resistance R_l.

$$G_A = \frac{P_{\text{A_OUT}}}{P_{\text{A_IN}}} = \frac{n \cdot (g_m V_g)^2 \cdot R_l/2}{n \cdot V_g^2/2R_g} = g_m^2 \cdot R_l \cdot R_g \quad (9)$$

where $P_{\text{A_OUT}}$ is the output power of the active block, as shown in Fig. 13, $P_{\text{A_IN}}$ is the input power of the same active block, and n is the number of combined transistors.

The drain efficiency η and power added efficiency PAE can be calculated as functions of P_{DC}, P_{out}, V_k, V_{dd}, n, and R_l. The dc power dissipation is constant in class-A operation, as the output power changes. Therefore, the drain efficiency as a function of output power P_{out} is given by

$$\eta = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{P_{\text{out}}}{n \cdot V_{dd} \cdot I_{dd}} = \frac{P_{\text{out}}}{n \cdot V_{dd} \cdot (V_{dd} - V_k)/R_l} \quad (10)$$

where I_{dd} is dc supply current to each transistor.

We can calculate the peak drain efficiency η_{MAX} from (7) and (10), as

$$\eta_{\text{MAX}} = \frac{n \cdot \dfrac{(V_{dd} - V_k)^2}{2R_l} \cdot \eta_{\text{out}}}{n \cdot V_{dd} \cdot (V_{dd} - V_k)/R_l} = \frac{1}{2}\left(1 - \frac{V_k}{V_{dd}}\right) \cdot \eta_{\text{out}} \quad (11)$$

$$\begin{aligned} \text{PAE} &= \eta \cdot \left(1 - \frac{1}{G}\right) \\ &= \frac{P_{\text{out}}}{n \cdot V_{dd} \cdot (V_{dd} - V_k)/R_l} \\ &\quad \cdot \left(1 - \frac{1}{\eta_{\text{in}} \cdot g_m^2 \cdot R_l \cdot R_g \cdot \eta_{\text{out}}}\right). \end{aligned} \quad (12)$$

B. Class-B Operation

Push–pull amplifiers operating in class-B mode can be analyzed to obtain closed-form solutions for the drain current and voltage waveforms by treating even and odd current harmonics separately. This is shown in the time-domain waveform of Fig. 15. The drain current waveform of a transistor operating in ideal class-B mode is composed of fundamental frequency and even harmonics only.

These currents can be calculated as follows:

$$\begin{aligned} I_{\text{D_EVEN}}(t) &= \frac{I_D}{2}\sin(\omega t) - \frac{I_D}{\pi}, \qquad 0 \le t < T/2 \\ I_{\text{D_EVEN}}(t) &= -\frac{I_D}{2}\sin(\omega t) - \frac{I_D}{\pi}, \qquad T/2 \le t < T \\ I_{\text{D_ODD}}(t) &= \frac{I_D}{2}\sin(\omega t) \end{aligned} \quad (13)$$

where T is the period and I_D is the peak drain current. These waveforms can be seen in Fig. 15.

The even harmonic components of the voltage waveform can be easily computed using the symmetry of the circuit. If the impedance of the transistor output capacitance is much less than Z_{Vdd}, the impedance seen by the even harmonic currents will be approximately that of the transistor output capacitance.

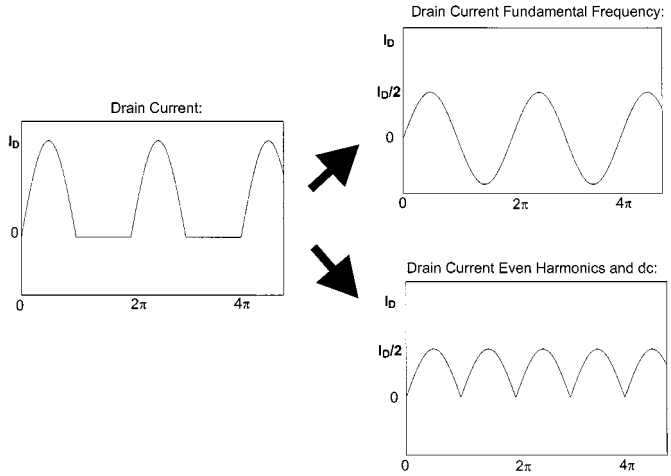

Fig. 15. Decomposition of the drain current waveforms into odd and even harmonics of a DAT amplifier operating in class-B mode.

Therefore, the even harmonic component of the drain voltage, $V_{\text{D_EVEN}}(t)$, can be calculated by integrating $I_{\text{D_EVEN}}(t)$, i.e.,

$$\begin{aligned} V_{\text{D_EVEN}}(t) &= -\frac{1}{C_d} \cdot \int_0^t \frac{I_D}{2}\sin(\omega t) - \frac{I_D}{\pi} \cdot dt \\ &= -\frac{I_D}{2\omega C_d}\left((-\cos(\omega t) + 1) - \frac{2\omega}{\pi}t\right), \\ &\quad 0 \le t < T/2 \\ V_{\text{D_EVEN}}(t) &= -\frac{1}{C_d} \cdot \int_{T/2}^t -\frac{I_D}{2}\sin(\omega t) - \frac{I_D}{\pi} \cdot dt \\ &= -\frac{I_D}{2\omega C_d}\left((\cos(\omega t) + 1) - \frac{2\omega}{\pi}t\right), \\ &\quad T/2 \le t < T. \end{aligned} \quad (14)$$

The fundamental component of the voltage can be computed by multiplying the fundamental component of the drain current by the resistance R_l presented by the output network. As in the class-A case presented in Section IV-A, we assume that the output network is adjusted so that this impedance is purely real.

$$V_{\text{D_ODD}}(t) = -\frac{I_D \sin(\omega t) \cdot R_l}{2}. \quad (15)$$

The actual voltage waveform can be found by superimposing the odd and even harmonic components, as shown in Fig. 16

$$V_D(t) = V_{\text{D_EVEN}}(t) + V_{\text{D_ODD}}(t) + V_{DD}. \quad (16)$$

It is noteworthy that the transistor output capacitance is essential to this mode of operation and cannot be ignored. Without this capacitance, the amplifier cannot operate in class-B mode since there would be no path for the even components of the drain current to flow through. Furthermore, if the transistors and these capacitors are small, the even component of the drain voltage becomes large and might damage the transistors, as depicted in Fig. 16. If the optimal transistor size has too small of an output capacitance, additional lumped capacitances can always be added.

In class-B operation, the maximum output power will be lower than that of class-A, as the even harmonics of the drain

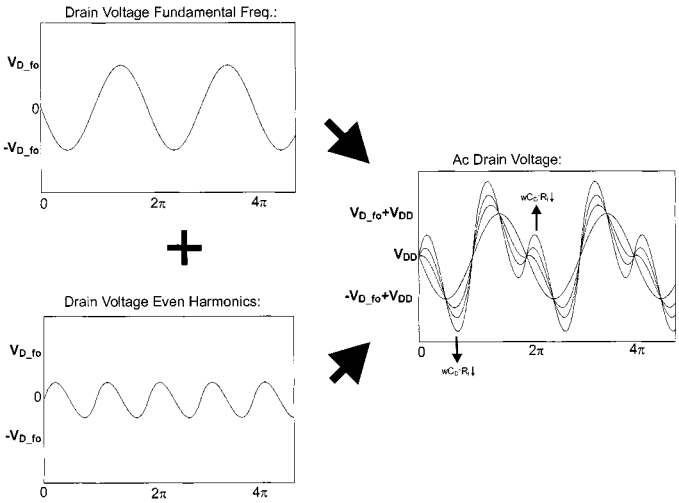

Fig. 16. Composition of the drain voltage waveform from odd and even harmonics of a DAT amplifier operating in class-B mode.

voltage will increase the maximum value of the drain voltage. This peak voltage can be calculated numerically from (15) and (16). The maximum allowable drain voltage component at the fundamental frequency is the difference between V_{dd} and V_k. If the even voltage peaks are small enough to be neglected, the output power $P_{\rm out}$ is the same as for class-A under same conditions, i.e.

$$P_{\rm out} = n \cdot \frac{(V_{dd} - V_k)^2}{2R_l} \cdot \eta_{\rm out}. \tag{17}$$

An example of the drain waveform for $\omega Cd \cdot Rl = 0.5$, 0.3 and 0.2 can be seen in Fig. 16.

The gain of the active block G_A for this mode of operation can be calculated as follows:

$$G_A = \frac{P_{\rm A_OUT}}{P_{\rm A_IN}} = \frac{n \cdot \left(\frac{g_m V_g}{2}\right)^2 \cdot R_l/2}{n \cdot V_g^2/2R_g} = \frac{g_m^2 \cdot R_l \cdot R_g}{4}. \tag{18}$$

The gain under conditions described by (18) will be 6 dB lower than the gain of the class-A operation. The gain of actual amplifier will be even lower since the transistor transconductance in the class-B operation is lower than that under class-A. The total power gain can be computed using (8).

Combining (9) with (18), we notice that the drain efficiency η and PAE can be calculated as functions of $P_{\rm out}$, $P_{\rm DC}$, V_{dd}, n, and R_l. The dc power dissipation $P_{\rm DC}$ is proportional to I_D in class-B operation, therefore

$$\eta = \frac{P_{\rm out}}{P_{\rm DC}} = \frac{P_{\rm out}}{n \cdot V_{dd} \cdot I_D/\pi} = \frac{P_{\rm out}}{n \cdot V_{dd} \cdot \frac{2}{\pi}\sqrt{2\frac{P_{\rm out}}{n \cdot \eta_{\rm out} \cdot R_l}}}$$
$$= \pi \cdot \frac{\sqrt{P_{\rm out} \cdot R_l \cdot \eta_{\rm out}}}{2\sqrt{2n} \cdot V_{dd}}. \tag{19}$$

It is interesting to notice that in both class-A and class-B cases the drain efficiency can be kept higher when output power is low if we can change either R_l or V_{dd} or both dynamically as $P_{\rm out}$ changes. Equations (10) and (19) clearly show this fact.

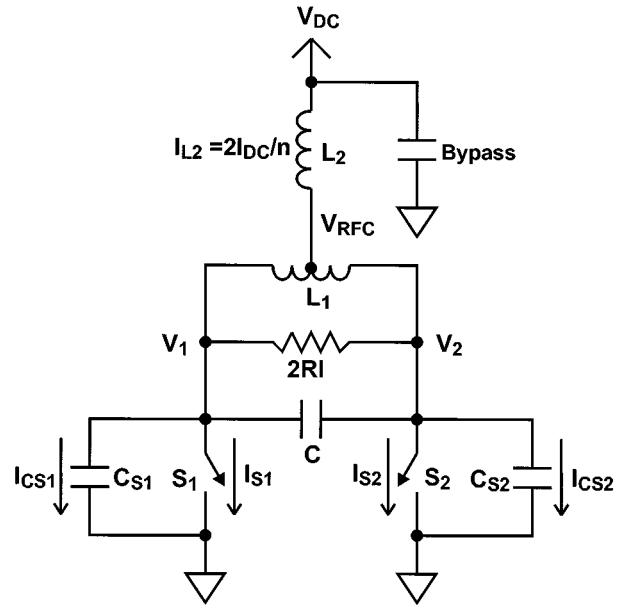

Fig. 17. Equivalent circuit of a push–pull class E/F$_{\rm odd}$ power amplifier with transistors operating substantially as switches.

We can calculate the peak efficiency $\eta_{\rm MAX}$ from (17) and (20), if the peaking in the drain voltage caused by even harmonic components is negligible, i.e.

$$\eta_{\rm MAX} = \frac{\pi}{4} \cdot \left(1 - \frac{V_k}{V_{dd}}\right) \cdot \eta_{\rm out}. \tag{20}$$

Finally, PAE can be determined using (12) and (20).

C. Class E/F$_{\rm odd}$ Operation

Class E/F$_{\rm odd}$ belongs to the recently introduced E/F family of zero voltage switching (ZVS) power amplifiers [14]. In this amplifier, the impedance seen by the transistor drain is the same as that of the class inverse F [16], [17] at every odd harmonic frequency and the same as that of class E for the fundamental and the even harmonics.

To analyze class E/F$_{\rm odd}$, the transistors should be approximated as switches with series resistance $R_{\rm on}$ [14]. This assumption is valid when the input power is high enough so that the transistor is either open or operates in the triode region during most of the cycle. The equivalent circuit may be seen in Fig. 17. There is no known simple solution to analyze the circuit when the transistor is operating part of the cycle as a current source and part of the cycle as an open or short circuit. Also, it is difficult to calculate the value of $R_{\rm on}$ analytically as a function of the input power and circuit parameters, since the transistor behavior during the transition from the open state to the short state and vice-versa is extremely nonlinear. This can be an interesting subject for future work. For this paper, we assume that $R_{\rm on}$ is constant for the input power above a certain value. This minimum input power and $R_{\rm on}$ may be extracted from numerical simulations of the amplifier.

The simple push–pull circuit of Fig. 17 can be used to provide virtual short circuits at the odd harmonics to each switch while leaving the impedance seen by the switches at the even

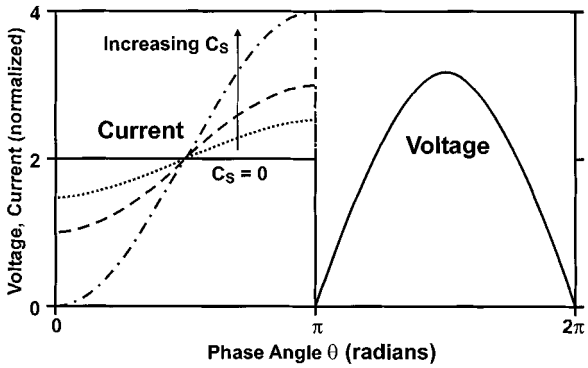

Fig. 18. Voltage and current waveforms of the switches of a class E/F_{odd} power amplifier. The change in the current waveform with increasing transistor output capacitance is depicted. The current on the plot does not include the current through this capacitance.

harmonics to be that of the switch output capacitance, as described in Section III-A. Furthermore, due to the symmetry of the circuit, the even harmonics are suppressed at the load, easing the task of filtering the output.

Initially, we assume the loss is negligible and the loaded Q of the resonator composed of L_1 and C is high. If this resonator is tuned near the fundamental frequency f_0, the voltage across it must be a sinusoid at that frequency. The resonator is then detuned to have the required inductance at the fundamental frequency to achieve ZVS conditions. The resonator should present between the transistor drains a reactance equal to that of each transistor's output capacitance, but with the opposite sign. Kirchhoff's voltage law requires that the voltage across the resonator be the same as the difference between the switch voltages, V_1 and V_2. In addition, V_1 and V_2 are zero during the half-period when the corresponding switch is closed. Therefore, the voltage across each switch must be half-sinusoidal, as in Fig. 18. For the dc voltage of this waveform to equal the supply voltage $V_{\rm DC}$, the peak voltage $V_{\rm pk}$ must be $\pi V_{\rm DC}$, i.e.

$$V_1 = \left\{ \begin{array}{cc} 0 & 0 \le t < T/2 \\ -\pi V_{\rm DC} \sin(\omega t) & T/2 \le t < T \end{array} \right\} \tag{21}$$

$$V_2 = \left\{ \begin{array}{cc} \pi V_{\rm DC} \sin(\omega t) & 0 \le t < T/2 \\ 0 & T/2 \le t < T \end{array} \right\}. \tag{22}$$

The currents I_{CS1} and I_{CS2} through the output capacitors C_{S1} and C_{S2} may be found using the known switch voltages, i.e.

$$I_{CS1} = \left\{ \begin{array}{cc} 0 & 0 \le t < T/2 \\ -\pi\omega C_{S1} V_{\rm DC} \cos(\omega t) & T/2 \le t < T \end{array} \right\} \tag{23}$$

$$I_{CS2} = \left\{ \begin{array}{cc} \pi\omega C_{S2} V_{\rm DC} \cos(\omega t) & 0 \le t < T/2 \\ 0 & T/2 \le t < T \end{array} \right\}. \tag{24}$$

If L_2 is large and conducts only dc current, for each half-cycle, one of the transistors is open circuited (and can be removed from the circuit), while the other is short circuited and conducts the excess current. Therefore, we can calculate the currents through the switches, I_{s1} and I_{s2}, as a function of amplifier total dc current $I_{\rm DC}$ as follows:

$$I_{S1} = \left\{ \begin{array}{cc} \dfrac{2I_{\rm DC}}{n} - I_{CS2} & 0 \le t < T/2 \\ 0 & T/2 \le t < T \end{array} \right\} \tag{25}$$

$$I_{S2} = \left\{ \begin{array}{cc} 0 & 0 \le t < T/2 \\ \dfrac{2I_{\rm DC}}{n} - I_{CS1} & T/2 \le t < T \end{array} \right\}. \tag{26}$$

The waveforms for the class E/F_{odd} amplifier with linear output capacitance, calculated from (21)–(26), are plotted in Fig. 18. A similar solution exists for nonlinear capacitors [14].

To calculate the amplifier total dc current, $I_{\rm DC}$, we can equate the fundamental frequency component of the square current through the switches to twice the current through the load. This will result in

$$I_{\rm DC} = \frac{n}{2} \left(\frac{V_{\rm DC}}{R_{\rm on} - \dfrac{4R_l}{\pi^2}} \right). \tag{27}$$

The instantaneous power loss is the product of $R_{\rm on}$ and its rms current. The average power loss is then given by

$$\begin{aligned} P_{\rm loss} &= n \frac{1}{2\pi} \int_0^{2\pi} I_{s1}(\theta)^2 \, d\theta \cdot R_{\rm on} \\ &= n \frac{1}{2\pi} \int_0^{\pi} \left(2I_{\rm DC}/n - \frac{\pi}{X_{CS1}} \right. \\ &\quad \left. \cdot \left(V_{\rm DC} - \frac{2I_{\rm DC}}{n} \cdot R_{\rm on} \right) \cos(\theta) \right)^2 d\theta \cdot R_{\rm on} \\ &= n \frac{R_{\rm on}}{2} \left(\left(\frac{2I_{\rm DC}}{n} \right)^2 \right. \\ &\quad \left. + \frac{\left(\dfrac{\pi}{X_{CS1}} \left(V_{\rm DC} - \dfrac{2I_{\rm DC}}{n} \cdot R_{\rm on} \right) \right)^2}{2} \right). \end{aligned} \tag{28}$$

To account for loss, the series resistance of the switch $R_{\rm on}$ and the voltage drop associated with it are included in (28).

Since the amplifier is saturated, the output power is no longer a function of the input power, but is instead a function of supply voltage $V_{\rm DC}$. We can calculate the approximate output power of the circular geometry amplifier as follows:

$$P_{\rm out} = (P_{\rm DC} - P_{\rm loss})\eta_{\rm out} = (V_{\rm DC} I_{\rm DC} - P_{\rm loss})\eta_{\rm out}. \tag{29}$$

As $P_{\rm out}$ is not a function of $P_{\rm in}$, the gain can be calculated using (28).

$$G = \frac{P_{\rm out}}{P_{\rm in}} = n \cdot \frac{\left(\pi \cdot \left(V_{\rm DC} - \dfrac{2I_{\rm DC}}{n} \cdot R_{\rm on} \right) \right)^2}{8R_l P_{\rm in}} \cdot \eta_{\rm out}. \tag{30}$$

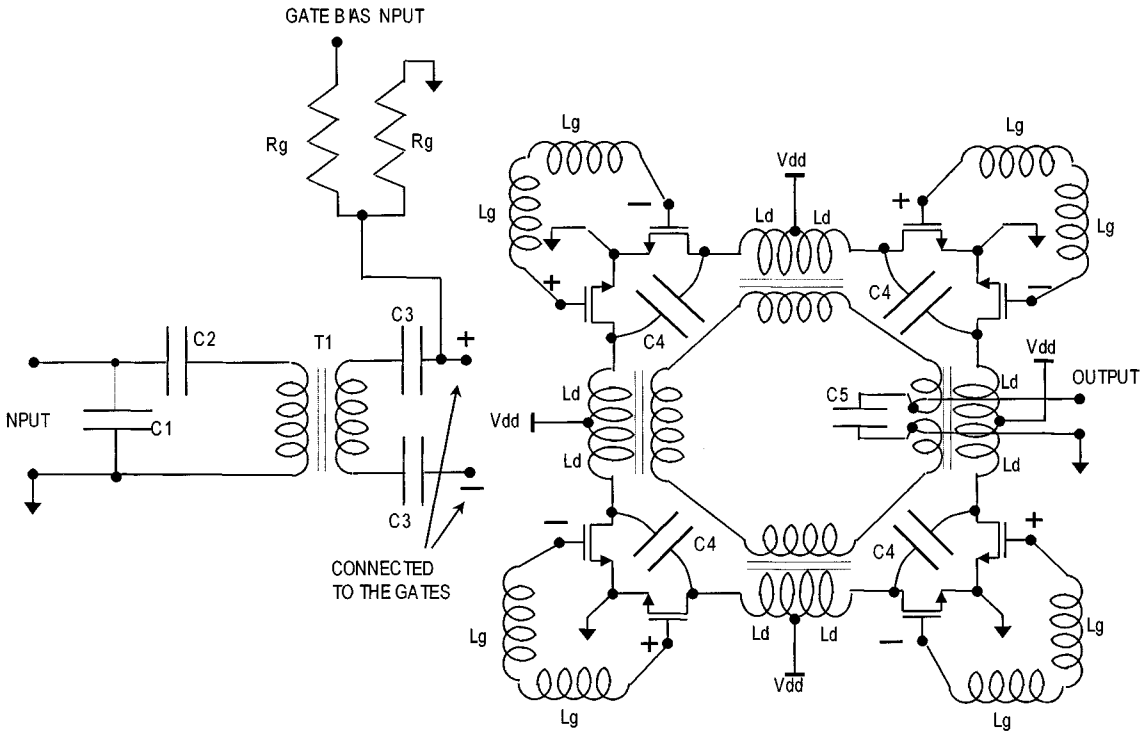

Fig. 19. Electrical diagram of a complete DAT amplifier with four push–pull blocks.

The drain efficiency may be computed using (27) and (28) to be

$$\eta = \left(1 - \frac{P_{\text{loss}}}{V_{\text{DC}} I_{\text{DC}}}\right) \cdot \eta_{\text{out}}. \tag{31}$$

Finally, the PAE may be obtained from (12), (30), and (31).

V. Experimental Results

As a demonstration of the concept, a 2-W 2.4-GHz single-stage fully integrated DAT switching power amplifier in class E/F_3 has been fabricated and measured using 0.35-μm CMOS transistors in a BiCMOS process technology. This process offers three metal layers, the top one being 3-μm thick with a distance of 4.3 μm from the substrate, the substrate has a resistivity of 8 Ω·cm. The chip area is 1.3 mm $\times$ 2.0 mm including pads. The complete electrical diagram of the designed circuit and a microphotograph of the chip can be seen in Figs. 19 and 20. Quasi-3-D simulation using SONNET [18] and circuit simulation using ADS [19] have been performed on the complete structure as a part of the design cycle to verify the performance of the amplifier.

In our measurement, the chip is glued directly to a gold-plated brass heat sink using conductive adhesive to allow enough thermal dissipation. The chip ground pads are wire bonded to the heat sink. The input and output are wire bonded to 50-Ω microstrip lines on printed circuit board. Supply and gate bias pads are also wire bonded. The input is driven using a commercial power amplifier connected to the circuit input through a directional coupler to measure the input return loss. The output is connected to a power meter through a 20-dB attenuator and 2.9-GHz low-pass filter to avoid measuring harmonic signal powers. All measurement system power losses

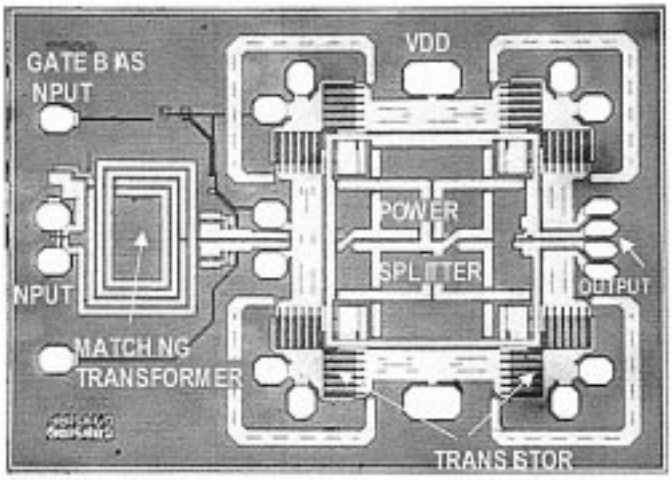

Fig. 20. Microphotograph of the first fabricated 2-W DAT power amplifier at 2.4 GHz using 0.35-μm CMOS technology.

are calibrated out, including the connector and Duroid board losses. The bond-wire power loss is included in the amplifier's measured performance.

Driving a balanced load, an output power of 1.9 W at 2.4 GHz is obtained with 8.7-dB gain using a 2-V power supply. The corresponding PAE is 41% and drain efficiency η is 48%. The amplifier can also drive a single-ended load, achieving a PAE of 31% with P_{out} of 2.2 W (33.4 dBm), gain of 8.5 dB, and drain efficiency of 36%. It can also produce 450 mW using a 1-V supply with a PAE of 27%. Figs. 21–23 show the gain and PAE versus output power for 2-V supply with differential output, 2-V and 1-V supplies with single-ended output, respectively. Small signal gain biased for class-A is 14 dB and input reflection coefficient is -9 dB. The 3-dB bandwidth is 510 MHz centered at

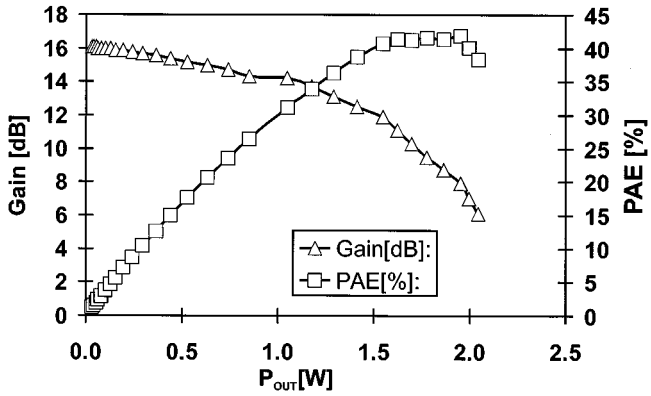

Fig. 21. Measured PAE and gain versus output power of the DAT amplifier operating with 2 V at 2.4 GHz with 50-Ω balanced output.

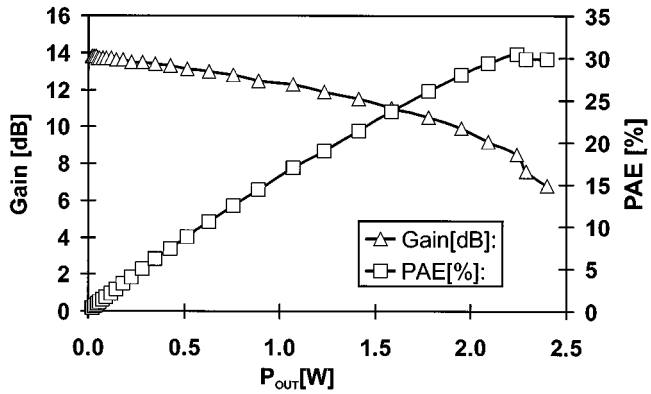

Fig. 22. Measured PAE and gain versus output power of the DAT amplifier operating with 2 V at 2.4 GHz with 50-Ω unbalanced output.

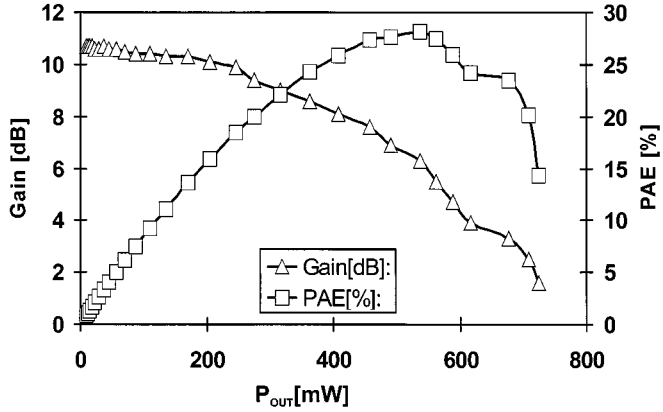

Fig. 23. Measured PAE and gain versus output power of the DAT amplifier operating with 1 V at 2.4 GHz with 50-Ω unbalanced output.

2.44 GHz. All harmonics up to 20 GHz were more than 64 dB below the fundamental in the absence of the output filter.

Using the transistor parameters obtained from the HSPICE transistor model ($R_{\rm on} = 0.6\ \Omega$ and $C_d = 6.1$ pF for $W = 900\times 10\ \mu$m) and output network parameters obtained from Sonnet EM simulation ($R_l = 7\ \Omega$, $\eta_{\rm out} = 0.7$), (29) predicts output power of $P_{\rm out} = 33.9$ dBm, and (31) predicts drain efficiency of $\eta = 53\%$. The simulation predicts $P_{\rm out} = 34.1$ dBm, and $\eta = 48\%$.

The difference between the theoretical, simulated, and measured drain efficiencies may be due to the transistor drive imbalance caused by the asymmetric feedback from the output signal and difference in signal phase across the transistor area which is not accounted for in the simulation.

TABLE I
COMPARATIVE TABLE OF THE PERFORMANCES OF THE RECENTLY REPORTED INTEGRATED POWER AMPLIFIERS

Freq GHz	P_{out} W	Sup V	PAE %	Wirebond Inductor	External Comp.	Active Device	Ref.
1.9	1.0	2	41	YES	YES	CMOS	[1]
0.9	1.0	1.9	41	YES	YES	CMOS	[2]
0.9	5.0	4.5	59	NO	YES	Si Bipolar	[3]
1.9	1.4	2.5	55	NO	YES	Si Bipolar	[4]
0.9	0.2	5	49	NO	NO	SOI LDMOS	[5]
2.4	0.25	7	79	NO	NO	GaAs MESFET	[6]
5-6	1.7	12	70	NO	NO	GaAs MESFET	[7]
1.9	0.63	3	52	NO	NO	GaAs MESFET	[8]
0.9	0.085	3	30 (D)	NO	NO	CMOS	[9]
1.9	0.1	3	16 (η)	NO	NO	CMOS	[10]
2.4	0.45	1	27	NO	NO	CMOS	this PA
2.4	1.9	2	41 (D)	NO	NO	CMOS	
2.4	2.2	2	31	NO	NO	CMOS	

D- Differential load
η- Drain-efficiency

VI. CONCLUSION

A new method for implementation of a power amplifier in a low-voltage CMOS process was presented. A novel fully integrated single-stage circular geometry active-transformer (DAT) power amplifier implemented in a low-voltage CMOS process achieves 1.9-W output power with 41% (31% single-ended) PAE at 2.4 GHz. It can also be used as a 450-mW 2.4-GHz amplifier with 27% PAE using a 1-V supply. The circuit includes input and output matching to 50 Ω, requiring no external components. This new concept combines several push–pull amplifiers efficiently with an extensive use of virtual ac grounds and magnetic couplings. None of the bonding wires is used as signal path inductors, making the circuit insensitive to their exact value. This is the first reported *truly* fully integrated power amplifier to achieve over 1 W in the gigahertz range using a low-voltage CMOS process, as can be seen in Table I, summarizing the previous works.

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