A 24-GHZ ACTIVE PATCH ARRAY

Dai Lu, Milan Kovacevic, Jon Hacker and David Rutledge

Department of Electrical Engineering
California Institute of Technology
Pasadena, CA 91125

Abstract

This paper presents an active patch array designed at 24 GHz. It can be used as a front-end component for a phased array. A series resonant array structure is chosen which is compact and easy excite. With 5 elements, the array proved a 12-dB antenna gain. A power amplifier and a low noise amplifier are designed on a single GaAs chip (PALNA). Bias switch is used in the PALNA which greatly reduces the switch loss in normal transceivers and increases the efficiency. 20-dB small signal gain is achieved in both power amplifier and low noise amplifier. The active patch array is built by the combination of the patch array and PALNA. Small signal, power and noise measurement are carried out inside the aneichoic chamber. In the noise measurement, we use sources at normal temperature and 77K (LN_2) to extract the noise figure of the active antenna by Y factor method. The performance proved that the active antenna is working efficiently as both a transmitting and receiving antenna.

Key Words

Active antenna, PALNA (power amplifier and low noise amplifier)

I. Introduction

An active antenna is a structure which combines the active devices with passive antenna together to improve its performance or introduce functionality directly into the antenna. Such antennas are of increasing interests as system designers require increased functions and compact space [1]. Also, the new high-volume commercial applications such as wireless LAN and collision avoidance radars require low-cost and light weight solutions, and the high level of integration achievable with active antennas inherently fulfill these requirements. The phased array with phasing network embedded is a key component in the current and future WLAN application. With fast and adaptive beam scanning, the mobile computer can find its target (another mobile computer , access point or router) easily, which improves its efficiency and mobility (Figure 1).

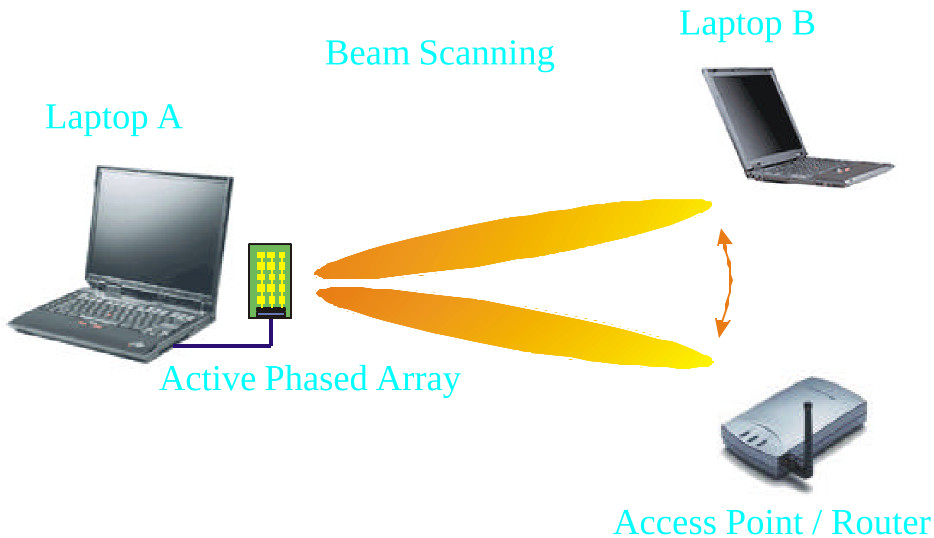


Figure 1 Phased array for the wireless LAN (WLAN)

In the past, the transmit / receive function in communications has usually been realized by separate modules connection, such as T/R switch, power amplifier and low noise amplifier. Even recently, these modules have been realized as separate MMIC chips, they still need to be connected by wire-bonding. Integration of these modules [2] into one MMIC chip can further reduce the size and cost. But practical realization seems to be a problem when the process for both low noise and power amplification is considered.

The GaAs PHEMT(Gallium Arsenide Pseudomorphic High Electron Mobility Transistor) has a well-established use as a high performance device which can work at frequencies up to W-band (75-110GHz)[3]. The combination of those terrific material properties, such as high mobility and low loss substrate, as well as property such as shot gates from fabrication techniques, i.e. Electron Beam Lithograph(EBL), determines its unique performance. Initially used for low noise amplifier applications, more recently GaAs PHEMTs have found applications in the low to medium power applications at millimeter wave frequencies with respectable power added efficiency [4]. So it is potentially a good candidate to integrate both power amplifier and low noise amplifier in a single chip. Actually, People have made some investigation on this problem before[5-6].

In this paper, both power amplifier and low noise amplifier are designed at 24 GHz. While the T/R switch loss is greatly reduced, the size of the whole module decreases to 2.3mm^2 (1.2x1.9mm). To make an active antenna, wire bonding is used to combine the PALNA and the patch. The performance of this active antenna is obtained by fully testing (small-signal, power and noise measurement) inside the aneichoic chamber. Combined with mixer, oscillator and A/Ds, this active antenna can be made an effective phased array element for 24GHz WLAN.

II. PALNA: power and low noise amplifier on the same chip

In this section, we will describe how we design the PALNA chip (Figure 2) and also show some of the measurement results. The amplifiers are designed in ADS using EE_HEMT1 transistor model for on-state simulations and S-parameter table based model for off-state simulations. The output impedance of the PA when biased off is purely inductive. Cascaded transmission line is added to the output of PA for the desired high-impedance state. This part of transmission line combines with LNA input for 50 ohm matching, while itself does not degrade the performance of the PA. There is another section of transmission line cascaded with LNA input for similar purpose. High isolation is provided between LNA and PA.

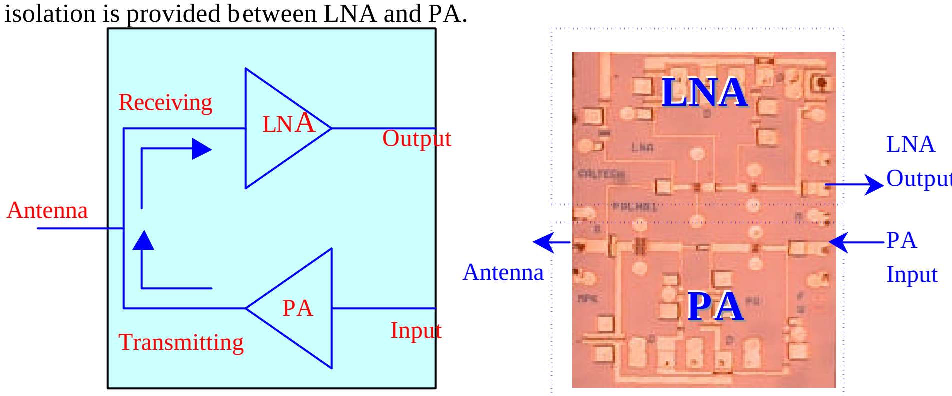
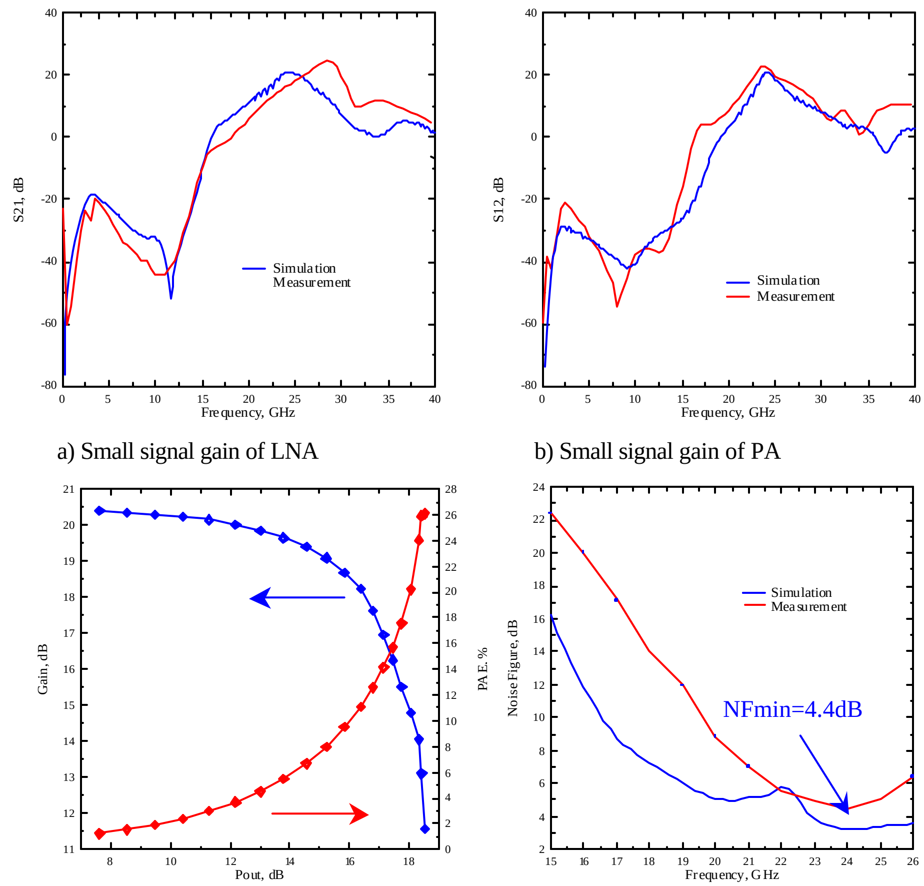


Figure 2 PALNA chip on GaAs PHEMT process

A two-stage (common source) topology is used for the LNA design, with the first stage matched for noise and the second stage matched for gain. Input, output and inter-stage impedance matching is accomplished by cascading and parallel transmission lines. A gate width of 80um is chosen for the trade-off between high gain and low noise. 2pF MIM capacitors are used for decoupling the DC and RF. Stability simulation is also carried out for DC to 30GHz and around 24GHz. In this design, we use source inductive degeneration for stabilization, impedance and noise matching. PA of this chip also has two stages. The first stage is optimized for gain and the second stage is designed to maximize the output power.

The PALNA chip was fabricated on a GaAs PHEMT process at Rockwell Science Center. Our design used the standard MMIC elements: microstrip lines, metal-insulator-metal (MIM) capacitors, ion-implant resistors, via holes for low impedance ground connection, two metal layers and air bridge crossovers. The GaAs wafer is 4-inch and 75um thick. The substrate material is grown by molecular beam lithograph (EBL). In order to achieve high breakdown voltage, gates were double recessed, with the final etch performed using plasma. The use of dry gate recess improved the uniformity of the devices to better than 5% across the entire wafer. The PALNA is approximately 1.2 by 1.9 mm in area.

The simulation and measurement results of this chip are shown below (Figure 3).



a) Small signal gain of LNA

b) Small signal gain of PA

c) Gain & PAE vs. Pout (PA)

d) Noise Figure (LNA)

Figure 3 Simulation and measurement of PALNA chip

As can bee seen from the plots, the chip works well in both transmitting and receiving. The small signal gain of LNA and PA are both above 20dB. But for LNA, the gain peaks at a little bit higher frequency of 28GHz. The shape of S12 and S21 agrees quite well between simulation and measurement. The output power goes up to 18dBm (63mW) and PAE maximum is 26%. A minimum 4.4dB noise figure is achieved at 24GHz. This noise performance of the LNA is not so great since we don’t have noise model for the transistor to be included during the period of noise simulation. The matching for LNA is –7dB and for PA is –4.5dB. The input impedance is designed intentionally capacitive to cancel the wire bonding effects, which also affect the noise measurement result of the chip.

III. Series resonant patch array

The series array configuration offers unique advantages to the microstrip antenna designers [7]. First, feed line lengths are greatly reduced, and thus reducing the radiation and dissipation losses which decrease array efficiency. Further, in larger arrays the high power lines are decoupled from those elements radiating lower power levels, which make the aperture distribution control quite tight.

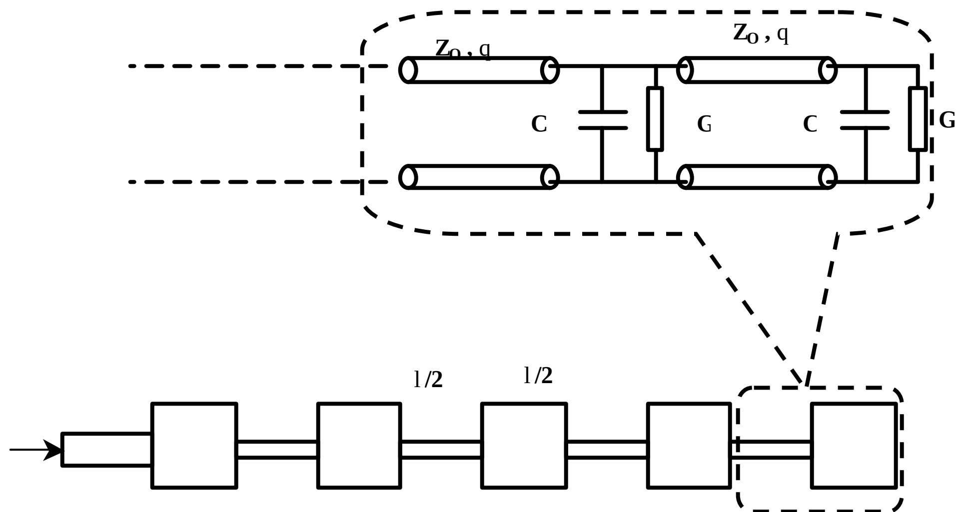


Figure 4 Transmission line model for the resonant microstrip array

The microstrip resonant array can be analyzed using the transmission line model as show in Figure 4. The radiation conductance can be calculated from the equivalent slot width, and the susceptance is the open-circuit capacitance of the low impedance line.

As can be seen from the model, the actual function of the cascading structure is like impedance transformer. And it transforms the high impedance at the edge of the square patch, which resonates at 24GHz, to a near 50 ohm for matching. As the number of elements increasing, we can also expect the impedance goes down and the gain of the antenna goes up. The simulation result by ADS Momentum is shown in Figure 5.a. All transmission-line model parameters can be calculated in the ADS schematic providing the S-parameters are known.

The microstrip patch array is made on Duroid with a low dielectric constant 2.2. The simulation gives about −15dB return loss at 24 GHz and 2% impedance bandwidth (S11< −10dB), while the measurement actually shows the resonant frequency shifting up to 24.31GHz with a better matching of −27dB. This shift may be due to the backside probe feed is not well characterized. The simulated and measured return loss are both shown in the Figure 5.b.

For this 1x5 patch array, we can expect a narrow E plane with 4 side lobes and a broad H plane (Figure 3). Some of the measurement results are summarized in Table 1. As we can see, there are sidelobes in measurement which are 2 dB higher than what is expected. This may be caused by the imperfection of the transition from back-side connector to microstrip on the board.

	Gain @24GHz	HPBW (E-plan	HPBW (H-plan	Sidelobe Level
Simulation	13.0 dB	17^{O}	74^{O}	-9.8 dB
Measurement	12.8 dB	16.1^{O}	66.8^{O}	-8.6 dB

Table 1 Summary of 1×5 patch array

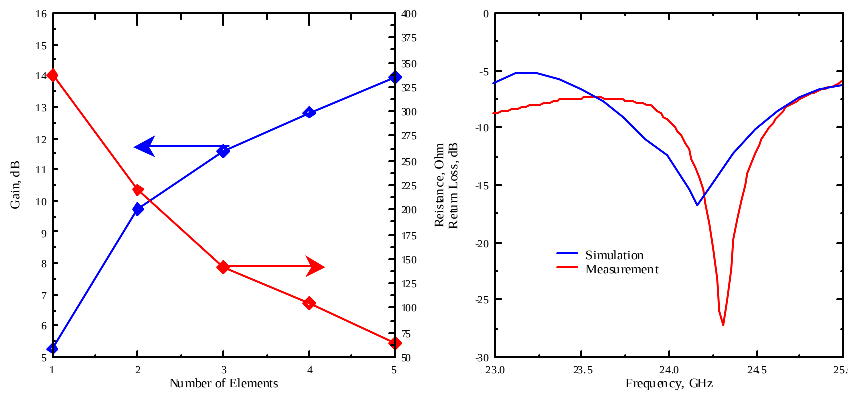


Figure 5 a) Resonant resistance and gain by array elements. b) Return loss of patch array

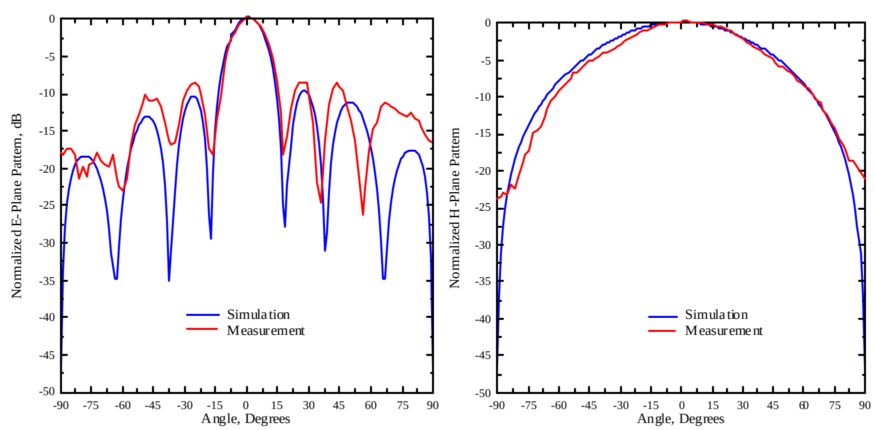


Figure 6 E and H plane pattern of 1x5 patch array

In simulation, the 1x5 patch array gives 12-dB gain at 24GHz. This is proved by measurement (Figure 7). If a high antenna gain and beam steering are required for applications such as WLAN, 2-dimensional patch array should be made. The author has built an 8x5 passive patch array with Wilkinson power combiner, which demonstrates a 21dB gain at 24GHz.

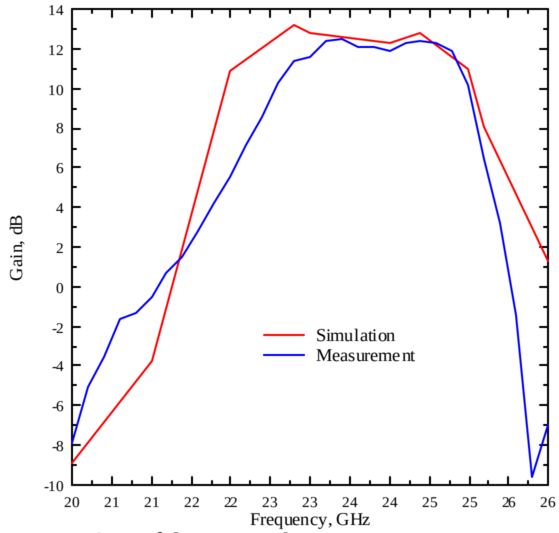


Figure 7 Gain of the 1x5 patch array

IV. Active antenna with PALNA

An active antenna is built by cascading the patch array with the PALNA chip (Figure 8). We use wire bonding to make the inter-connections between GaAs to the Duroid boards for both RF and DC signal transmission. Four DC Bias are used to switch the chip between transmitting and receiving states. The total size of the active patch array is 6x2.5 cm^2.

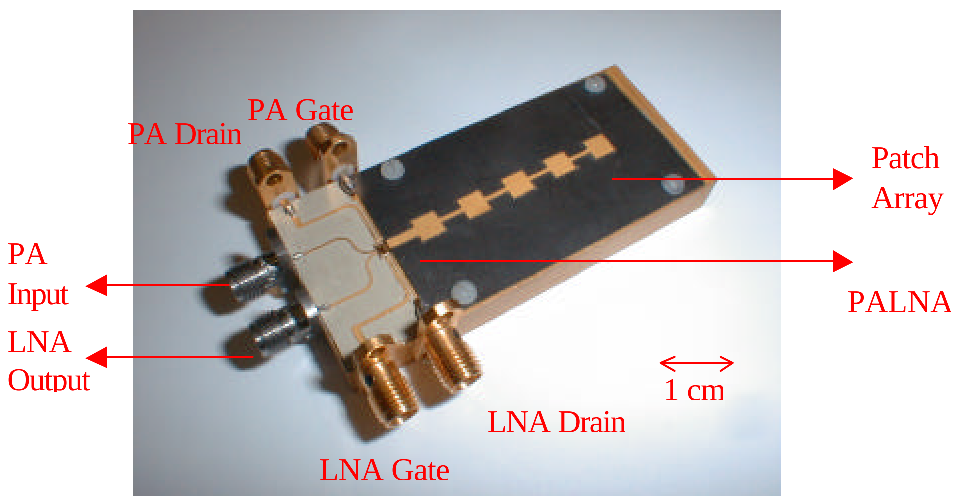


Figure 8 Active patch array with PALNA

4.1 *S-parameter Measurement*

Two-port S-parameter measurement inside the chamber gives the small signal performance of the active antenna. We use Friis transmission formula to extract the active gain of this antenna after de-embedding the radiation loss. Both of the transmitting and receiving measurements shows a gain peak at 24GHz, which is 20dB above the passive patch array (Figure 9). The active gain in transmitting mode is 3.5dB higher than in receiving mode. This may due to the better transition match between the PA than the LNA to the microstrip line.

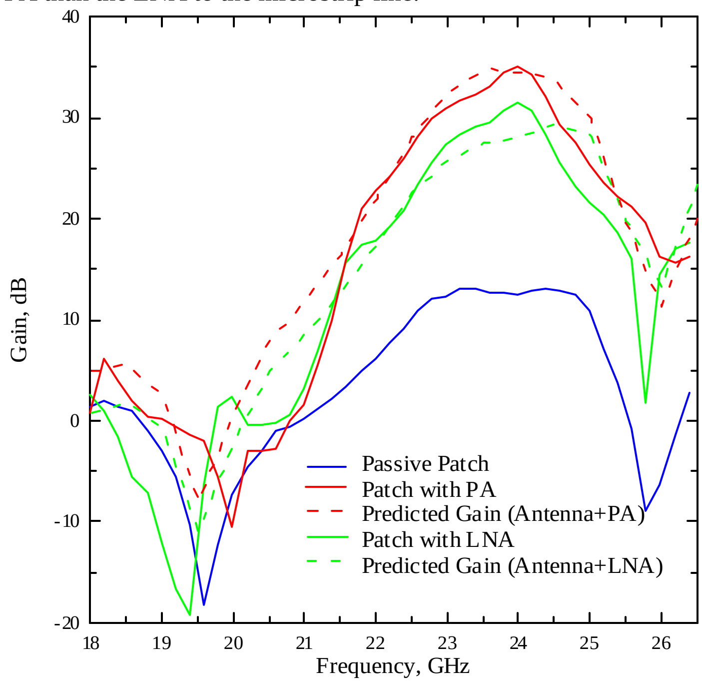


Figure 9 Gain measurement of passive and active patch

E and H plane pattern comparisons are made between passive and active patch antenna (Figure 10). The nulls in the E plane are almost in position but the sidelobe amplitude ratios have changed. It seems from the plot that a sidelobe level of 10 dB is reached for both transmit and receive modes, which is better than the original passive patch. The H plane pattern looks quite similar. There are a few small ripples at large angles in the transmit mode which may due to the connector loose caused by trembling effects during the turning of step motor.

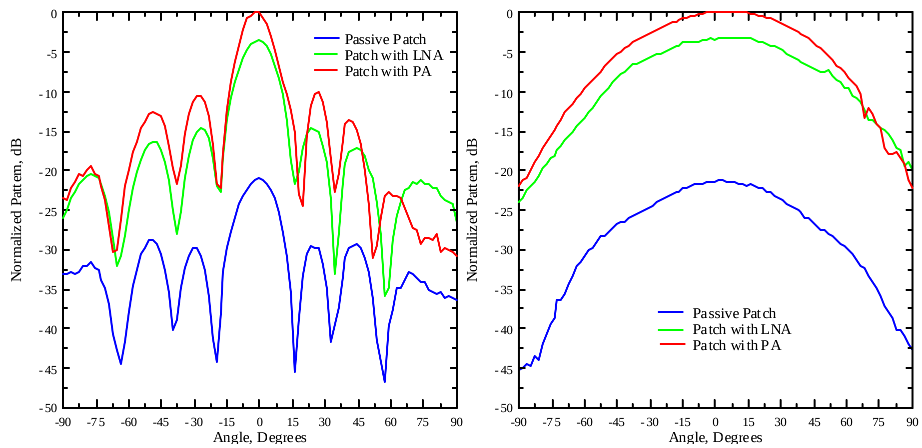


Figure 10 E and H plane of active and passive patch array

4.2 *Power measurement*

To see how the power amplifier works with the antenna, a power sweeping is done in the anechoic chamber. 1-dB and 3-dB compression points are identified in the plot (Figure 10). EIRP (equivalent isotropically radiated power) is used to characterize the performance of the radiation, which is defined by

$$EIRP = P_{rad} \cdot Gain$$

This is the power needed to feed in the isotropic radiator if the same amount of power is to be received. The maximum of EIRP of this active antenna can achieve is 34dBm=2.51W, which is reasonable high. If we assume 12dB for the passive patch, the maximum radiated power is 22dBm=158mW.

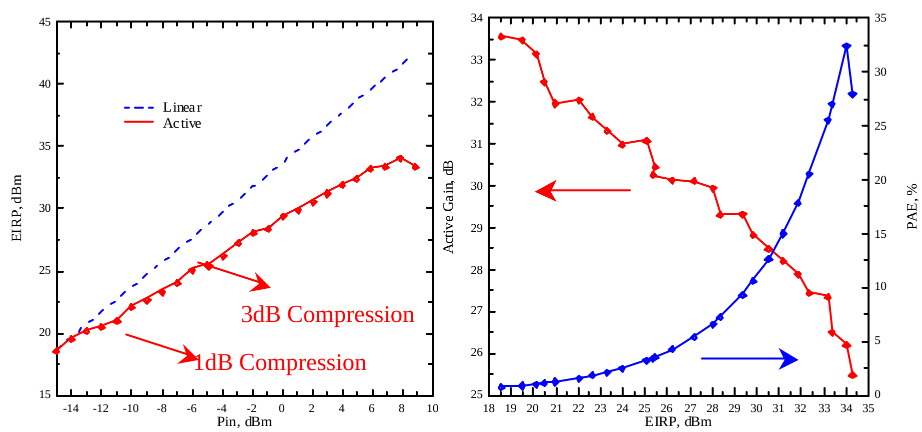


Figure 11 EIRP, active gain and PAE of the active patch array

Also PAE (power added efficiency) is calculated from the measurement data (Figure 11). The maximum PAE obtained is 32%, when the active gain drops at about 25dB. All the measurement is done at 24GHz.

4.3 *Noise measurement*

Noise figure is a very important performance factor for the receiver. The noise measurement has been done in the chip level, which gives about 4dB noise figure at 24GHz. This high noise value may partially due to the bad impedance matching to 50ohm. A more reliable noise measurement is done after inter-connection of the active device and antenna. The following setup (Figure 12) is used to do the do Y-factor noise measurement [8]. The active antenna is facing down inside Styrofoam box with absorber materials filled. The output of the LNA is amplified by another post-amplifier and then sent to the spectrum analyzer. The post-amplifier itself is a cascading of a solid state amplifier and an TWT amplifier, which provides an average 65dB gain across the 18-35 GHz band. This high amount of gain is necessary to bring the noise from LNA above the noise floor of the spectrum analyzer. The post-amplifier is calibrated before the measurement to obtain its noise figure and gain. When the active antenna is in receiver mode, two kinds of power are recorded in spectrum analyzer. One is at normal temperature, the other is made at 77K by pouring liquid nitrogen (LN_2) inside the box to make a cold radiating source. The power difference gives us the Y-factor. After de-embedding the noise of the post-amplifier, the noise figure of the active antenna is obtained (Figure 13). The noise figure of 3.51 dB at 24GHz is possible for use in the receivers.

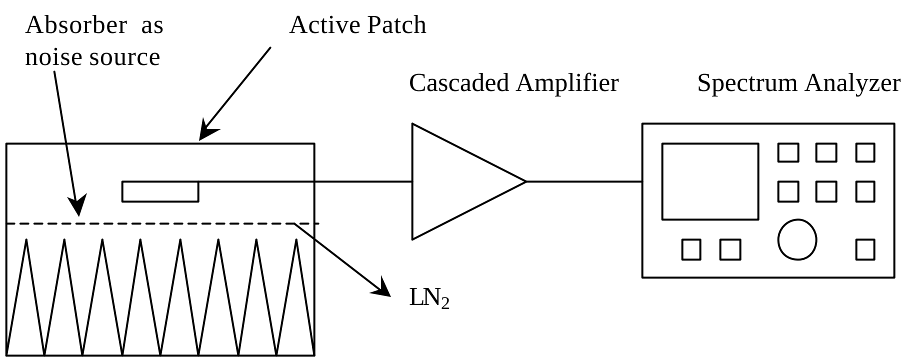


Figure 12 Measurement setup for the noise figure

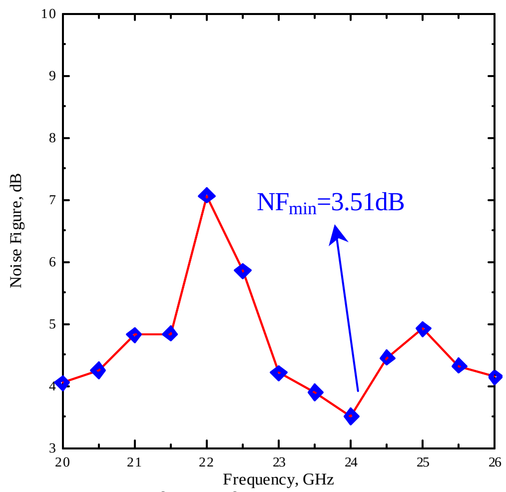


Figure 13 Noise figure of the active antenna in receiver mode

V. Conclusion

An active patch array is built for millimeter wave networks. The antenna shows a 20dB additional gain in both transmit and receive modes. The measurement gives a total radiated power maximum of 150mW and the PAE maximum of 32%. The noise figure is 3.51dB at 24GHz which makes this antenna quite promising for possible use in the phase array for WLAN.

Acknowledgements

We appreciate the support of the Lee Center for Advanced Networking at Caltech. The authors also want to thank Chun-Tung Cheung, Ichiro Aoki and Scott Kee for valuable discussion and help in the measurement.

Reference:

[1] Jenshan Lin, Tatsuo Itoh, "Active Integrated Antennas", *IEEE Trans. Microwave Theory Tech*., MTT-42, pp. 2186-2194, Dec. 1994.

[2] John R. Sellin, Stow; Donald N. Jessen, Sudbury, "Transmit and Receiver Switch", *US Patent*, No. 4,637,073, Jan. 1987.

[3] S. Weinreb, E. Fisher, B. Kane, N. Byer, M. Zimmerman, "W-band 0.3 W pHEMT MMIC power amplifier module," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium 1995*, pp. 25-28.

[4] Emilio A. Sovero, Youngwoo Kwon, Don S. Deakin, John Hong, "Watt Level GaAs PHEMT Power Amplifiers 26GHz and 40 GHz for Wireless Applications", *1999 RAWCON Digest*, pp. 309-312.

[5] Kevin W. Kobayashi, “An AlGaAs/GaAs HBT PA-LNA Transceiver MMIC Chip for 1.9 GHz PHS Digital Cordless Telephones”, *Microwave Journal*, Jan. 1998.

[6] K. Yamamoto, K. Maemura, N. Kasai, Y. Yoshii, Y. Miyazaki, M. Nakayama, “A Single-chip GaAs RF Transceiver for 1.9 GHz Digital Mobile Communication System”, *IEEE JSSC*, Vol.31, No.12, pp. 1964-1973, Dec. 1996.

[7] Thomas Metzler, “Microstrip Series Arrays”, *IEEE Trans. Antennas and Propagat.*, AP-29, pp. 174-178, Jan. 1981.

[8] Agilent Technologies , “Noise Figure Measurement Accuracy – The Y Factor Method”, *Application Note 57-2*.