21.7 A Fully Integrated 24GHz 8-Path Phased-Array Receiver in Silicon

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Available frequency spectrum, co-channel interference, and multi-path fading determine the data-rate limits of today's high-speed wireless communications. Higher frequencies offer more bandwidth, while enabling multiple antenna approaches by reducing the required antenna size and spacing.

Versatile multiple antenna systems provide a plethora of solutions for communications and radar, such as multiple-input-multiple-output (MIMO) diversity transceivers and synthetic aperture radars (SAR). Phased arrays constitute a special class of multiple antenna systems that imitate the behavior of directional antennas whose bearing can be adjusted via electrical means. Generally, a radiated signal arrives at spatially separated antenna elements at different times. Phased arrays compensate the time delays between the elements and combine the signals to enhance the reception from the desired direction, while rejecting emissions from other directions. Coherent addition of the signal and the uncorrelated nature of noise in an N-path phased array receiver improve the SNR by $10\log_{10}(N)$ [dB] at the array output.

The ISM band at 24GHz is a good candidate for broadband communications using multiple antenna systems with a small size. At 24GHz, a smaller delay spread exists compared to lower frequency bands (e.g. 2.4GHz and 5GHz bands) for indoor environments, allowing higher data rates [1]. In addition, a recent FCC ruling opens the 24GHz band to automotive radar applications, such as autonomous cruise control (ACC) [2].

In this work, we present a fully integrated 8-path phased-array receiver in silicon for the 24GHz ISM band. As mentioned earlier, the 8-path receiver improves the SNR by 9dB. For a narrowband signal, phase shifting can be done at various stages, namely, RF, LO, IF, analog baseband, or digital domain. Digital base-band phase shifting architectures are power hungry due to the large number of ADCs and high-speed DSP requirements. RF phase shifting was not pursued because of the large loss of integrated phase-shifters at 24GHz, mostly caused by passives. Large area is the main reason for discarding phase shifting at IF or analog baseband. Thus, we adopted LO-path phase shifting in this work.

Figure 21.7.1 shows the block diagram of the 24GHz, 8-path phased-array receiver. The receiver uses two-step down conversions with an IF of 4.8GHz, allowing both LO frequencies to be generated using one synthesizer loop and a divide-by-four. A single oscillator core generates 16 discrete phases providing 4-bits of phase resolution. A set of 8 phase-selectors (i.e. analog phase multiplexer) apply the appropriate phase of the LO to the corresponding RF mixer for each path independently. The operating state of the chip including phase-selection information (beam-steering angle) is serially loaded into an on-chip shift-register using a standard serial interface. The signal image at 14.4GHz is attenuated by the front-end's narrowband transfer function (i.e. the antenna and LNA). Two mixers driven in quadrature perform the second down conversion to baseband. The divide-by-four block generates the necessary I and Q phases of the second LO.

Each of the eight RF front-ends consists of two inductively degenerated common-emitter LNA stages in series followed by a double-balanced Gilbert-type mixer (Fig. 21.7.2). The input of the first LNA is matched to 50Ω, and the subsequent blocks of the front-end are power matched for maximum power transfer. We chose the transistor size and bias currents to simultaneously minimize the noise figure and achieve a power match. On-chip PTAT and band-gap references generate the bias currents and voltages, respectively.

The outputs of all eight mixers are combined in the current domain and terminated to a tuned load at the IF. A binary tree of on-chip transmission-lines provides symmetrical paths from the mixers' outputs to the tuned-load for current combining. The IF stage consists of a tuned amplifier centered at 4.8GHz followed by a pair of double-balanced Gilbert-type mixers driven by I and Q signals generated by the divide-by-4 block. Two baseband differential buffers drive the output.

The 16-phase 19GHz VCO is designed as a ring of eight differential CMOS amplifiers with tuned loads similar to the 4-stage implementation in [3]. Tuned loads facilitate the generation of the necessary phase-shifts of 22.5^{o} at frequencies close to the maximum operating frequency of the NMOS transistors. An integer-N frequency synthesizer is also implemented to control the center frequency of the VCO.

Each receiver path has independent access to all 16 phases of the LO. The LO phase selection for each path is done in two steps. Initially, an array of eight differential pairs with switchable current sources and a shared tuned load selects one of the eight LO phase pairs (Fig. 21.7.3). A dummy array with complementary switching signals maintains a constant load on the VCO buffers and prevents variations in phase while switching. Next, the polarity (the sign bit) of the LO is selected by a similar 2-to-1 phase selector providing all 16 LO phases. The aforementioned cascaded configuration reduces the number of phase selectors from 16 (i.e., 2^4) to 10 (i.e., 2^3+2) for each path. The cross-coupled differential pairs at the output of each stage partially cancel the loss associated with the inductors and transistors' outputs, increasing the LO amplitude driving the RF mixers. Each 16:1 phase selector consumes 12mA. A symmetric tree structure for all 16 phases transfers the LO signal to the phase selection circuitry of each path with minimal path mismatch.

The phased-array receiver is implemented in IBM 7HP SiGe BiCMOS technology with a bipolar f_T of 120GHz and 0.18μm CMOS transistors [4]. It offers five metal layers with a 4μm-thick top analog metal used for on-chip spiral inductors and transmission lines routing the high-frequency signals. The die micrograph of the phased-array receiver is shown in Fig. 21.7.7.

Figure 21.7.4 shows the measured transfer function of each receive path. To assess the array performance, an artificial wave front is generated by feeding the RF inputs of each receiver path via power-splitters and adjustable phase-shifters. Figure 21.7.5 shows the normalized array gain as a function of signal incident angle at three different LO-phase settings for four-path operation. It clearly demonstrates the programmable spatial selectivity of the phased-array receiver. Figure 21.7.6 summarizes the receiver's measured performance.

References:

[1] D. Lu et al., "Investigation of Indoor Radio Channel from 2.4GHz to 24GHz," *IEEE AP-S Int. Symp. Dig. Papers*, pp. 134-137, June 2003.

[2] Federal Communications Commission, FCC 02-04, Section 15.515.15.521.

[3] J. Savoj et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit With a Half-Rate Binary Phase-Frequency Detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 13-21, Jan. 2003.

[4] A. Joseph et al., "A 0.18μm BiCMOS Technology Featuring 120/100GHz (f_t/f_{max}) HBT and ASIC-Compatible CMOS Using Copper Interconnect," *BCTM Proceedings*, pp. 143-146, 2001.

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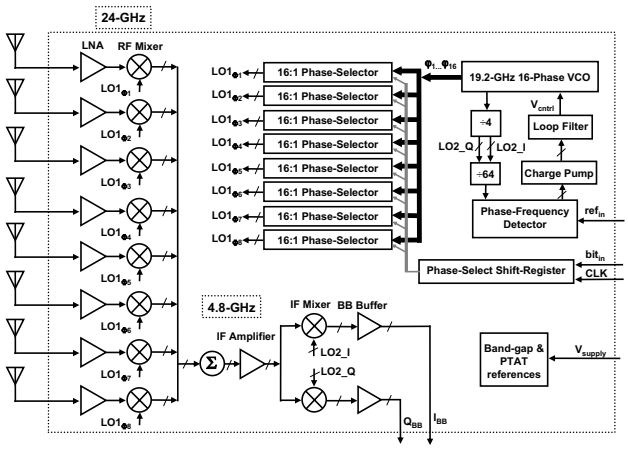

Figure 21.7.1: Block-diagram of the 24GHz phased-array receiver.

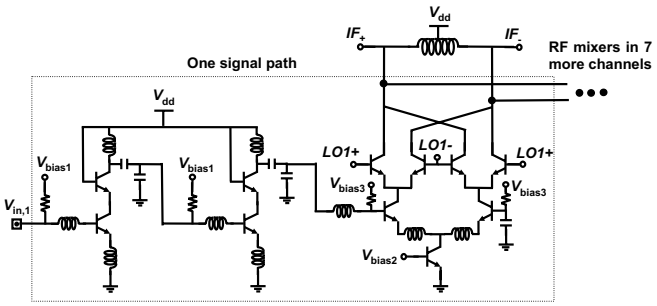

Figure 21.7.2: Schematics of the 24GHz front-end (one path).

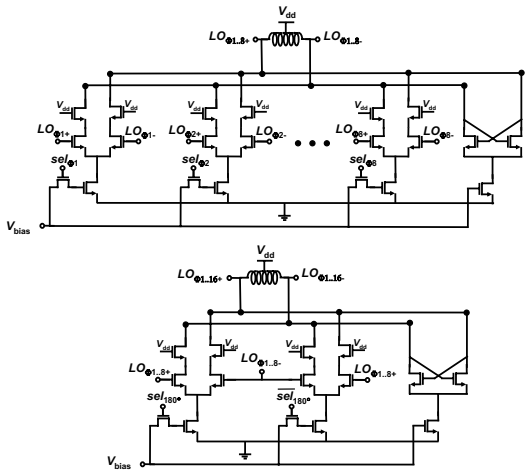

Figure 21.7.3: Schematics of LO phase selection circuitry for each path: an 8:1 analog multiplexer (dummy replica array not shown) followed by a sign selector.

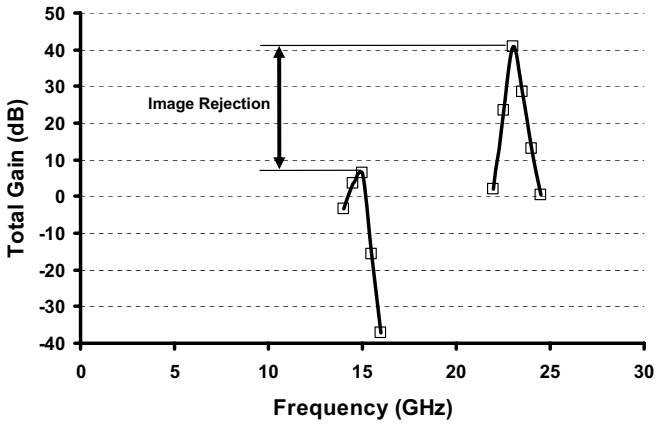

Figure 21.7.4: Receiver small-signal transfer function (one path) for the main and image signals.

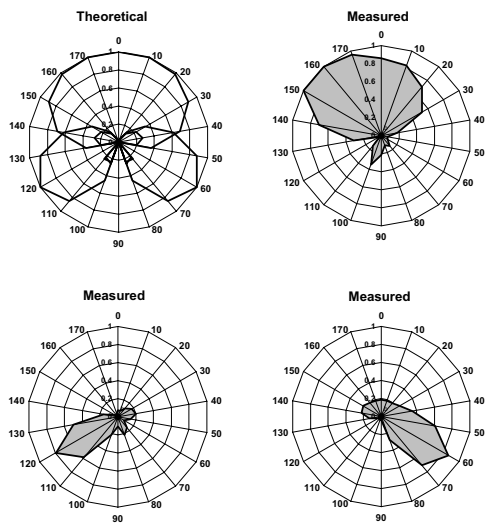

Figure 21.7.5: Measured pattern of a 4-path array at different incidence wave angles compared to the theoretical predictions (ideal case).

Signal Path Performance (per path)	
Peak Gain	43dB
Noise-Figure	8.0dB
Input-Referred 1dB Compression Point	-27dBm
Input-Referred 3rd-Order Intercept Point	-11.5dBm (2 tones 5MHz apart)
On-chip Image Rejection	35dB
Current Consumption [*RF (each path)* / *IF*]	12mA (RF)/ 12mA (IF)
S_{11}	< -10dB
LO Path Performance	
VCO tuning range	18.79GHz – 20.81GHz (10.2%)
K_{VCO}	2.1 GHz/V @19.2GHz
VCO Phase-Noise	-103dBc/Hz @ 1MHz offset
Current Consumption (VCO + buffers)	59mA
Complete Receiver Performance (8 paths)	
Total Array Gain	61dB
SNR Improvement	9dB
Beam-forming Resolution	22.5°
Beam-forming Peak-to-Null Ratio	20dB (measured for 4 paths)
Power Dissipation @ 2.5V	364mA 287mA (w/o biasing and baseband buffers)
Technology	SiGe, 120GHz HBT, 0.18µm CMOS
Die Area	3.5mm x 3.3mm

Figure 21.7.6: 24GHz phased-array receiver performance summary.

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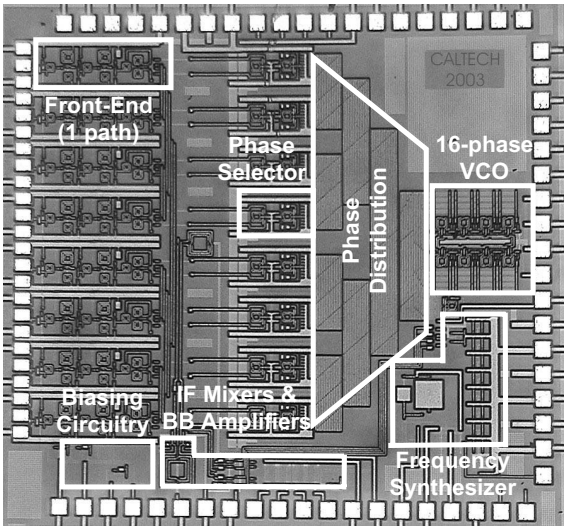
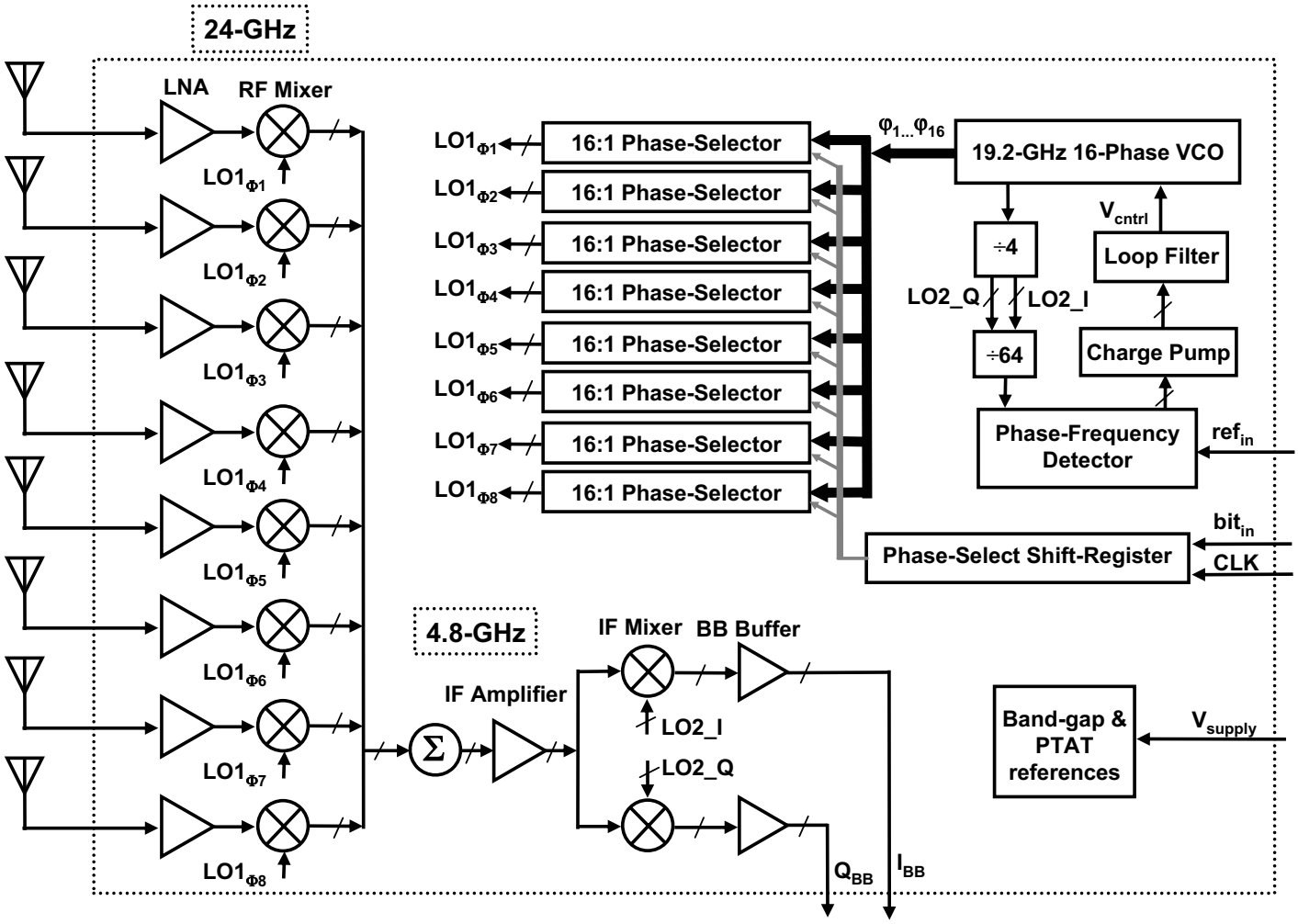


Figure 21.7.7: Die micrograph of the 24GHz phased-array receiver.



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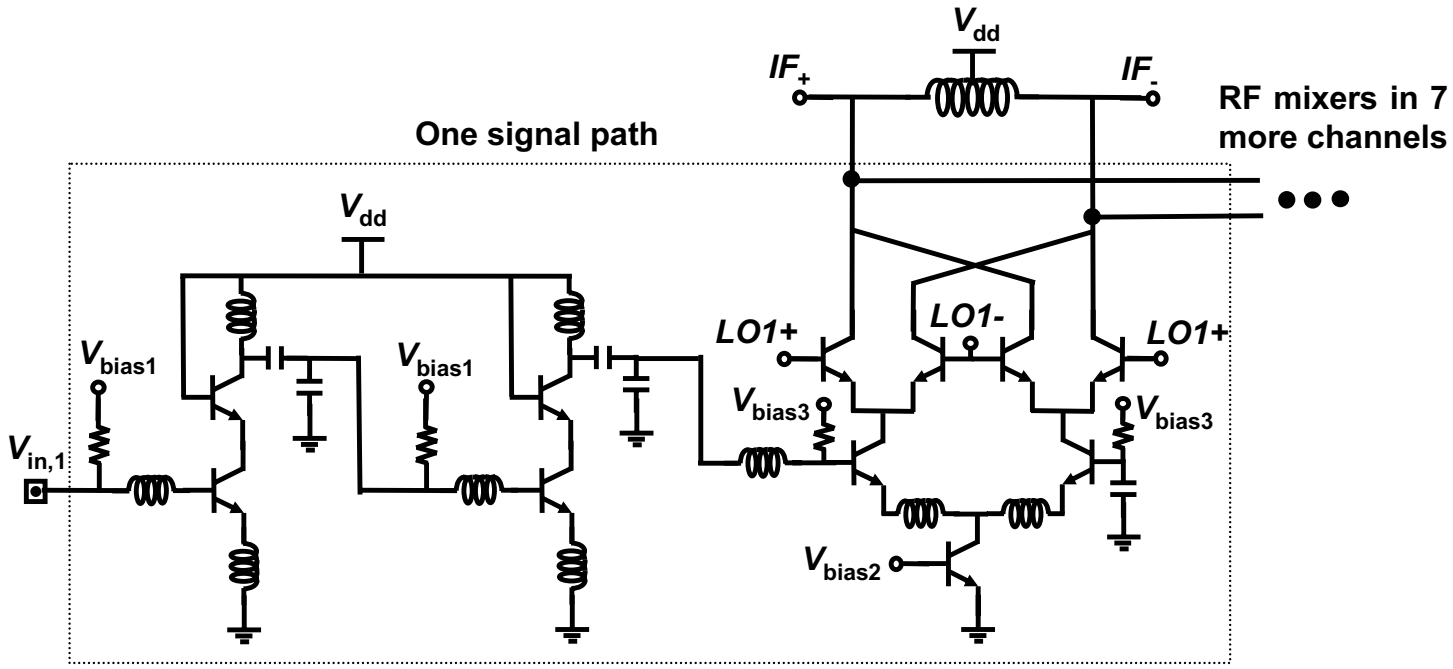

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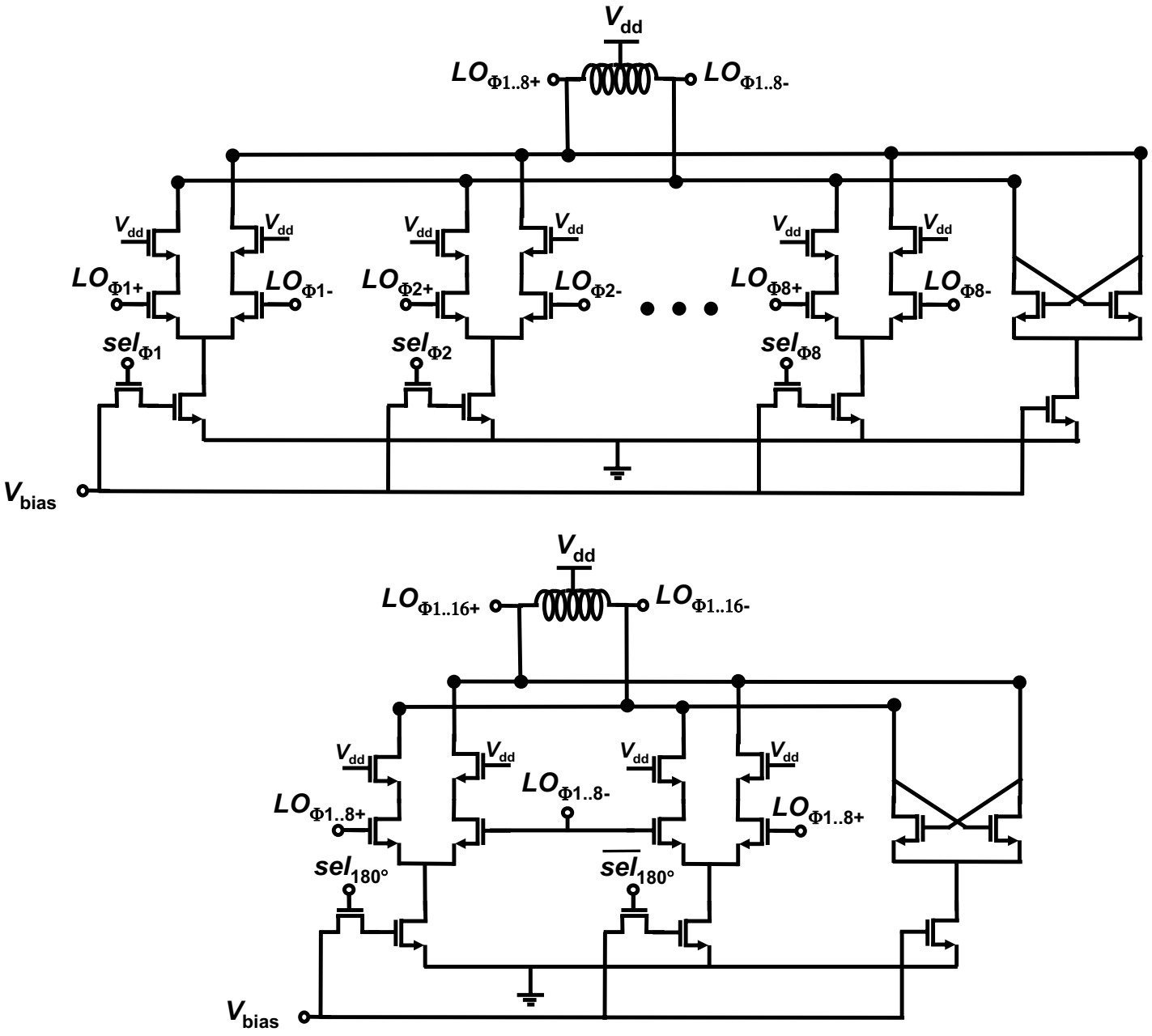

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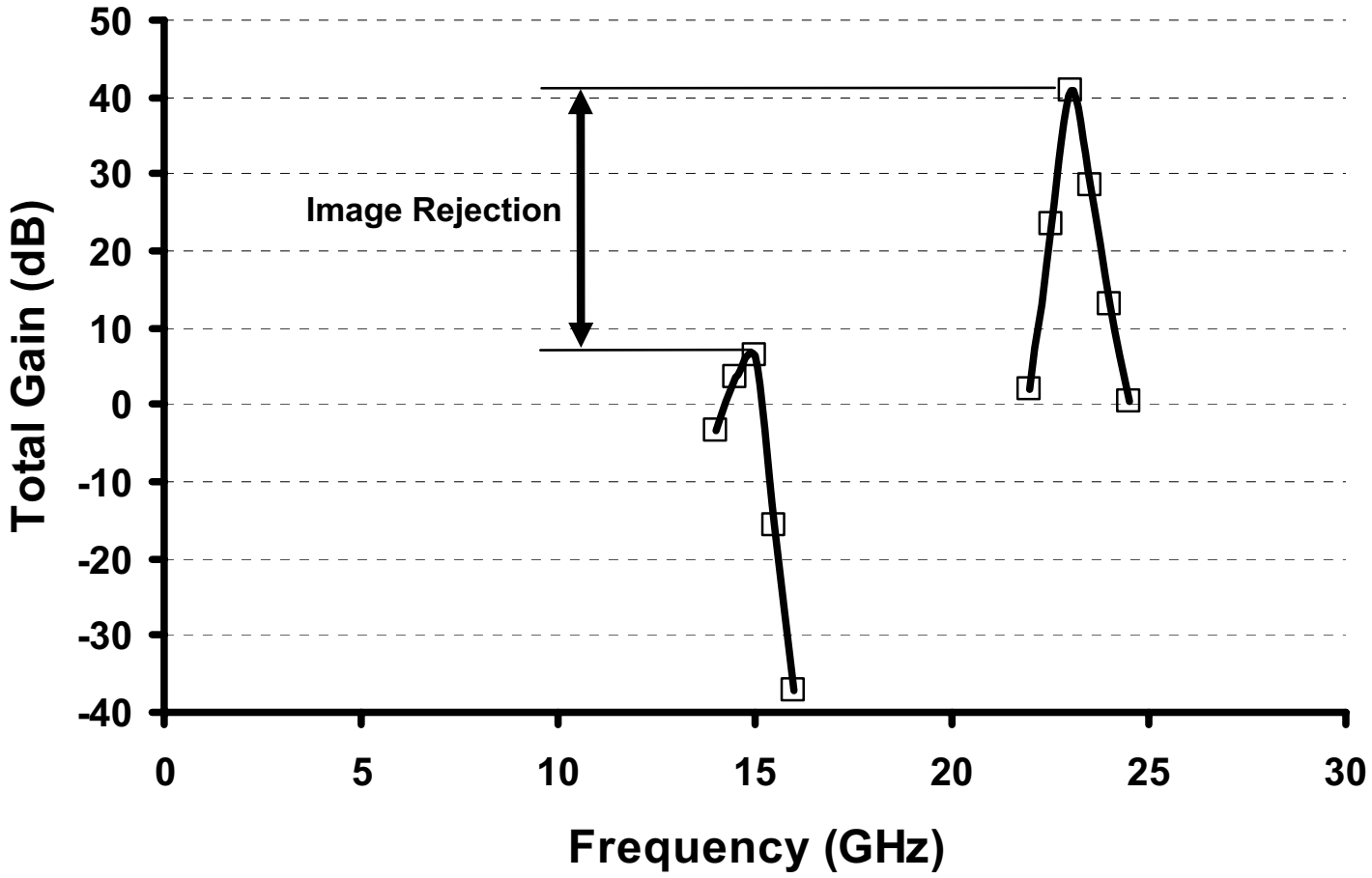

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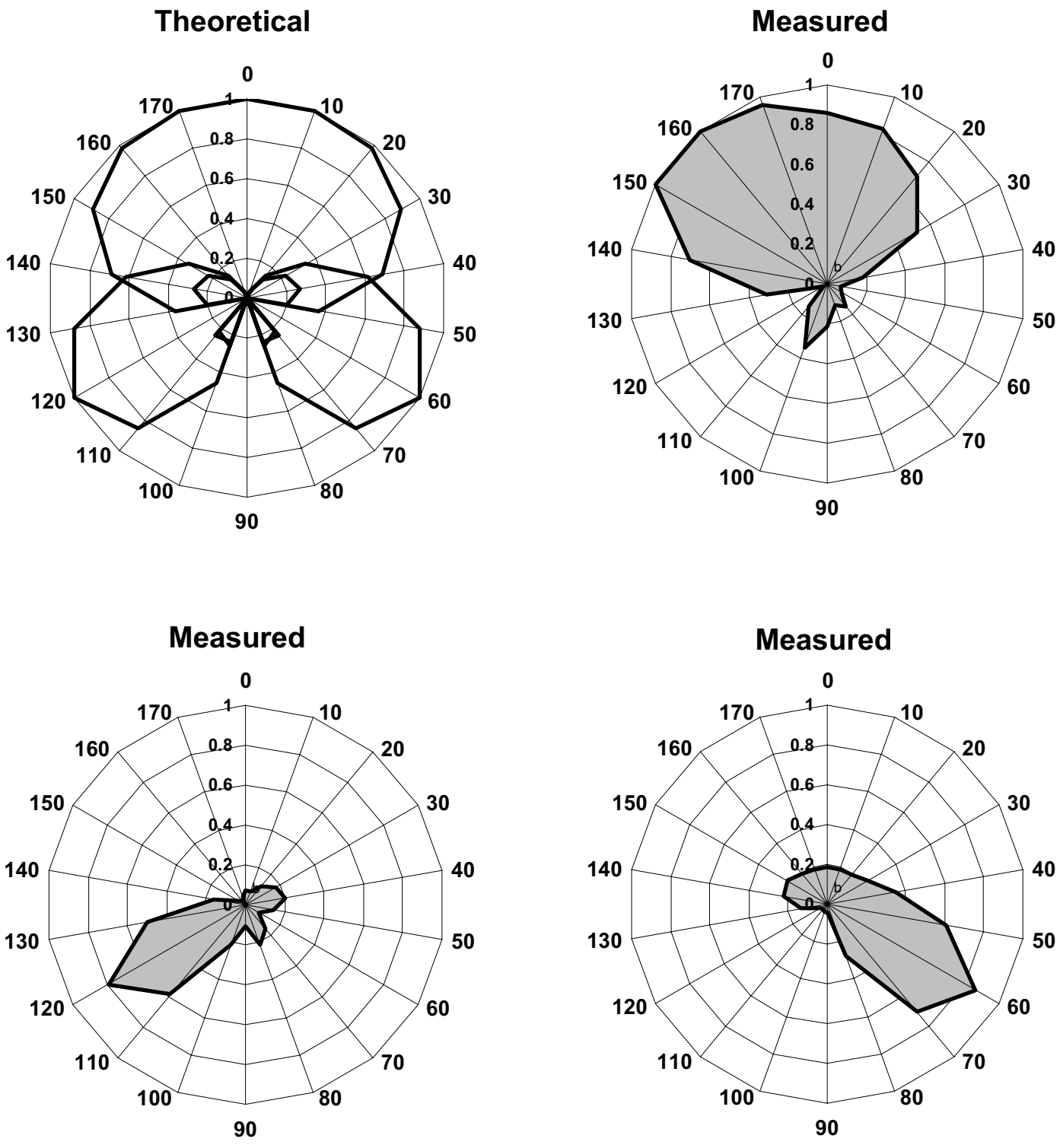

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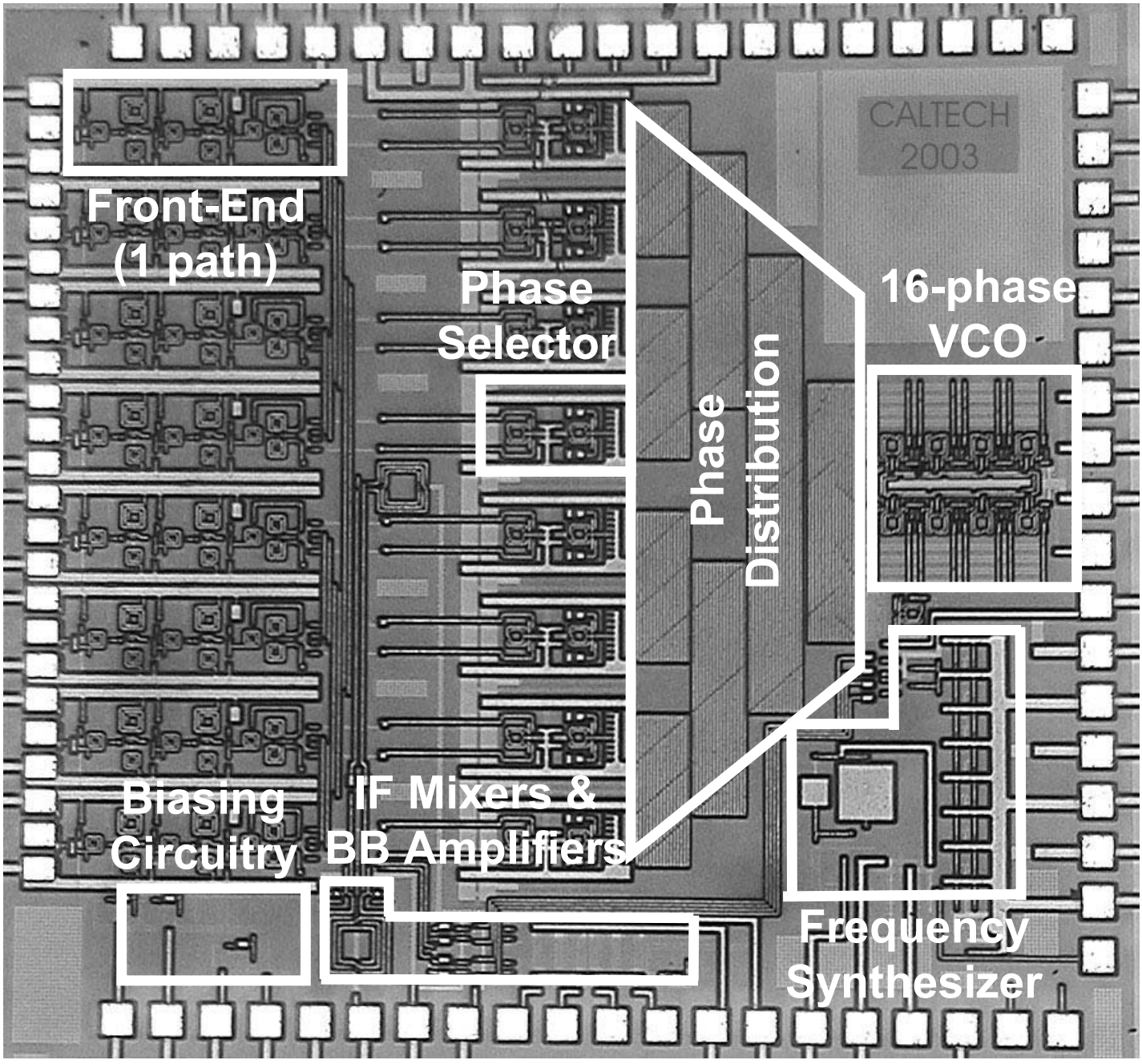

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